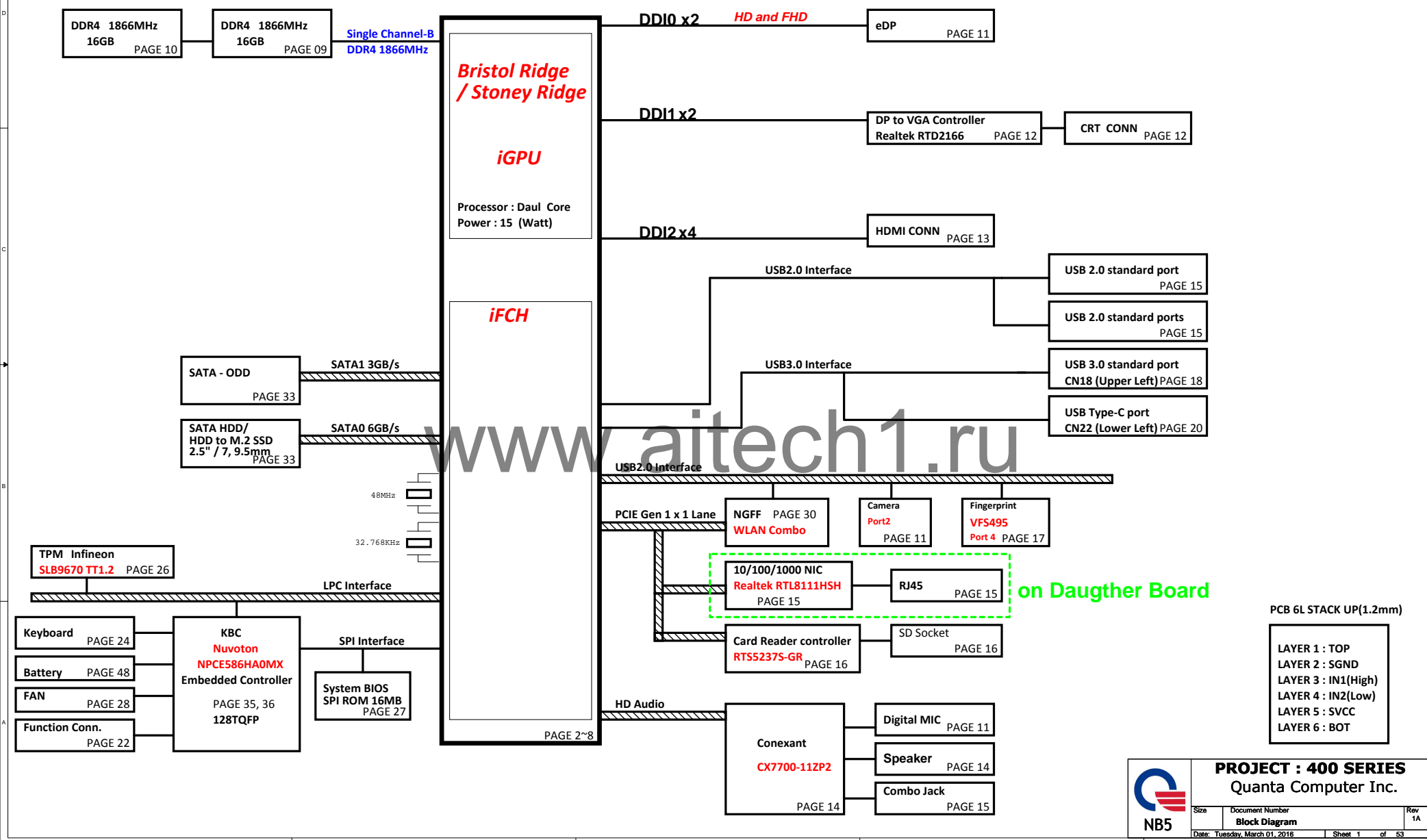
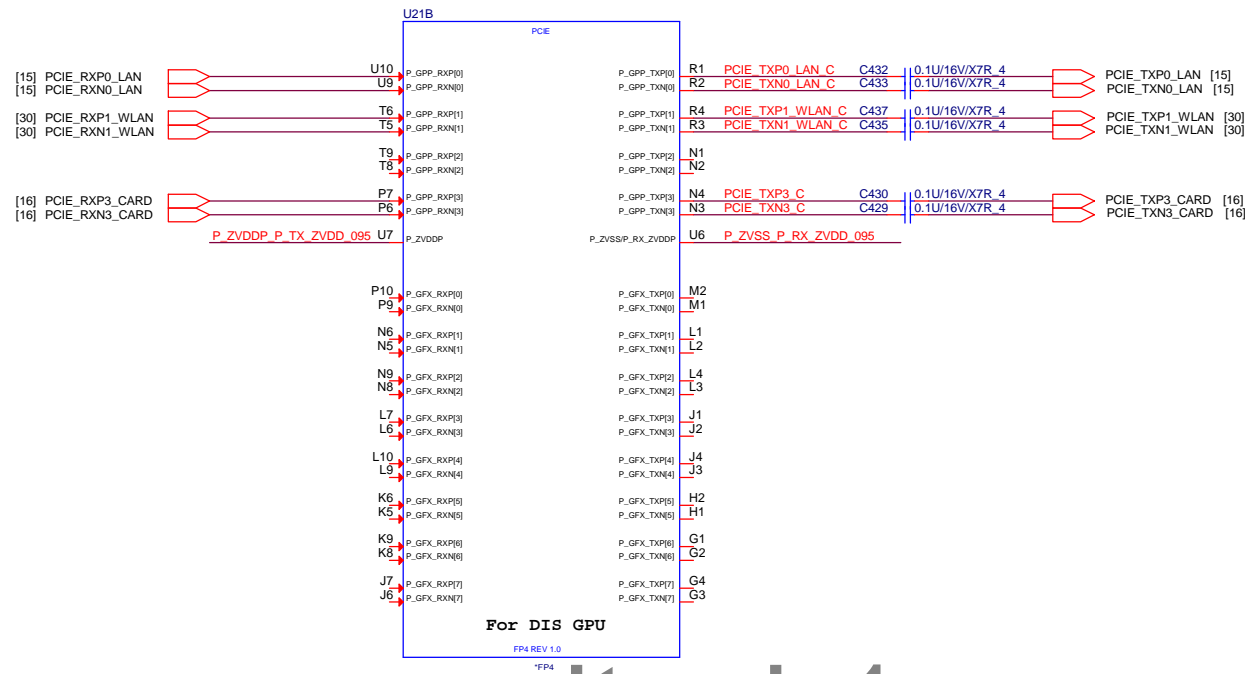
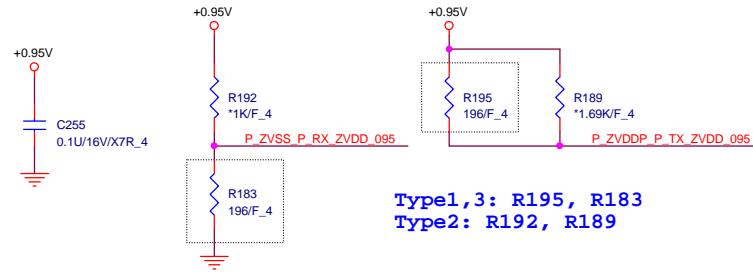


01



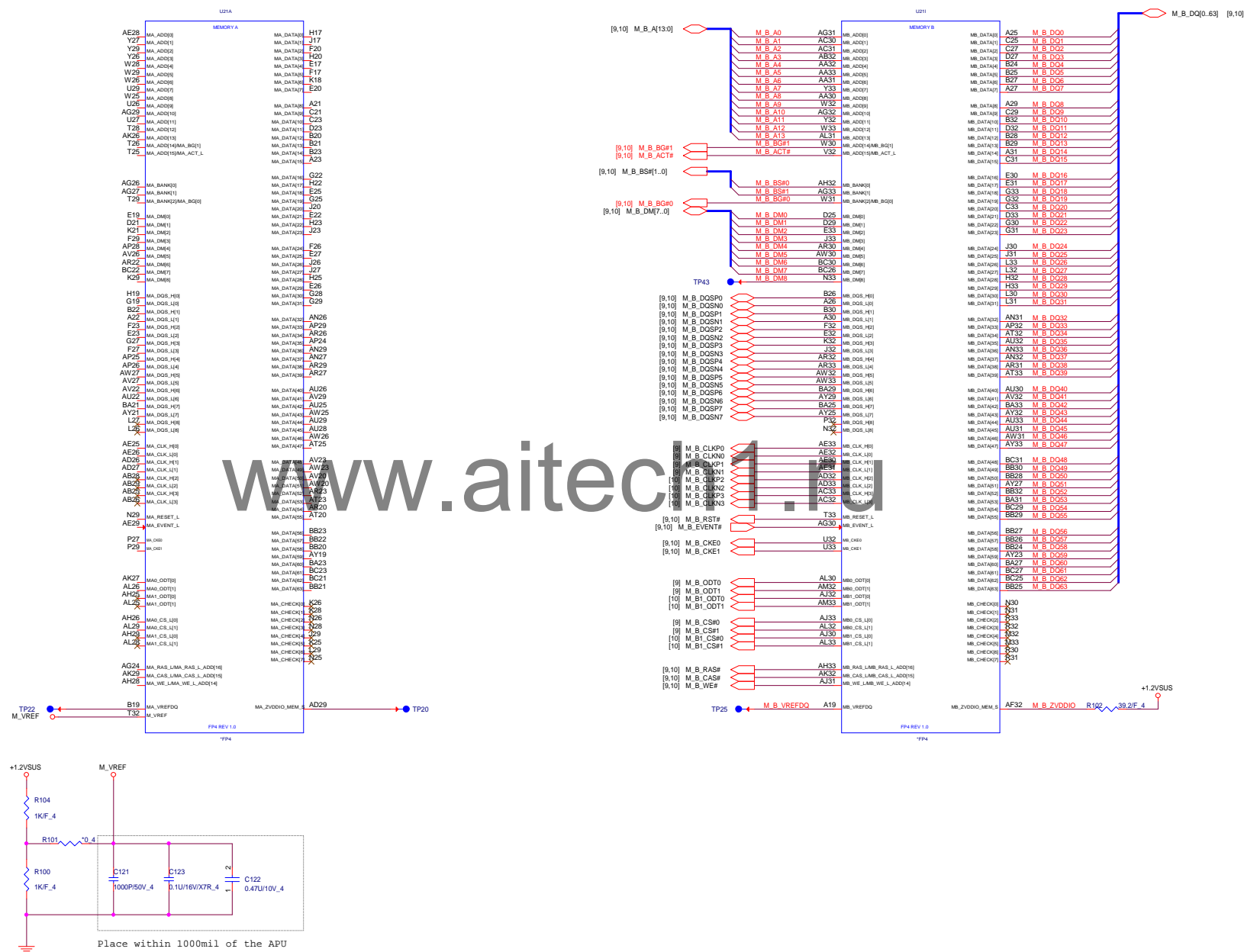


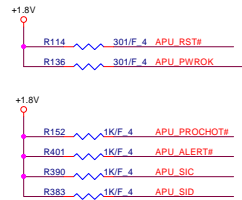
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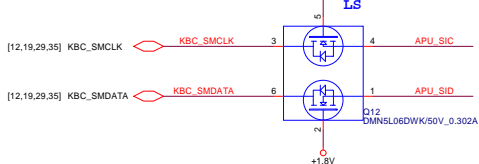
PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
	BR/ST 1/7 (PCIe)	1A
Date: Tuesday, March 01, 2016	Sheet 2 of 53	

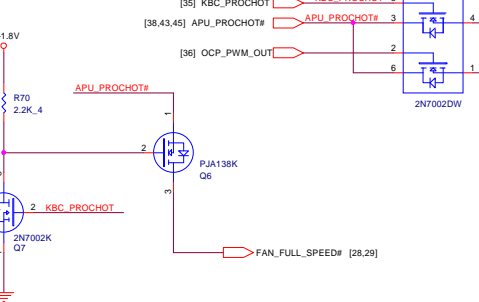




Type1/3: LS, 1.8V
Type2: LS, 3.3V

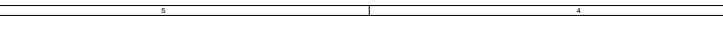
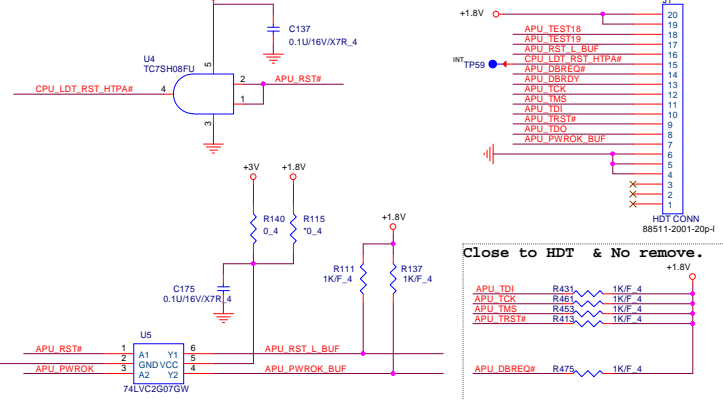


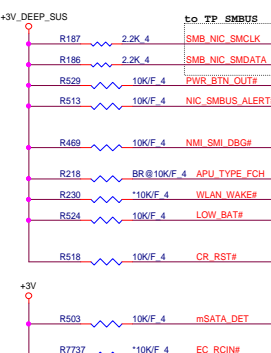
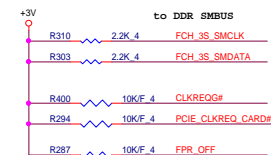
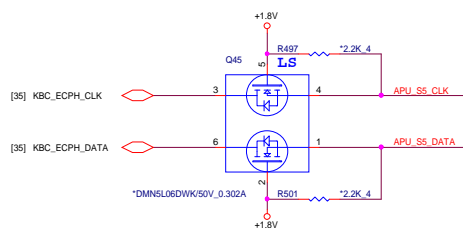
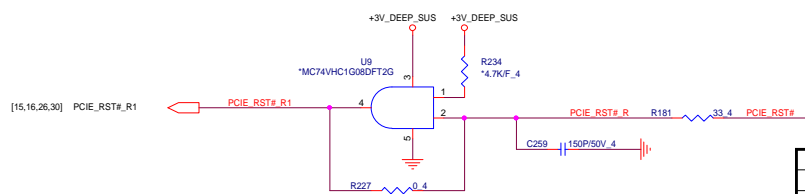
APU_PROCHOT# Signal Level:
Type1/3: +1.8V
Type2: +3.3V



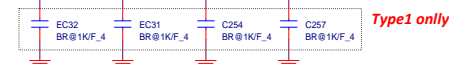
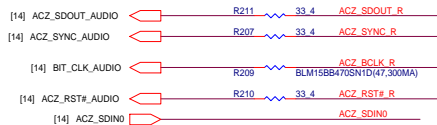
HDT+ Connector for Debug only

Can remove on MP

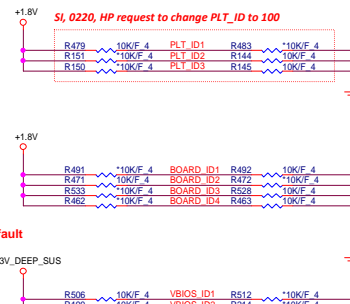




To Azalia

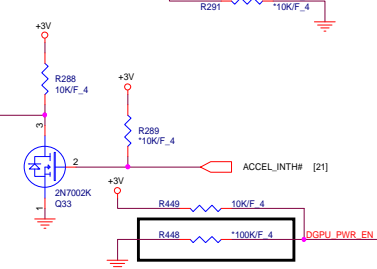
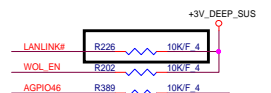
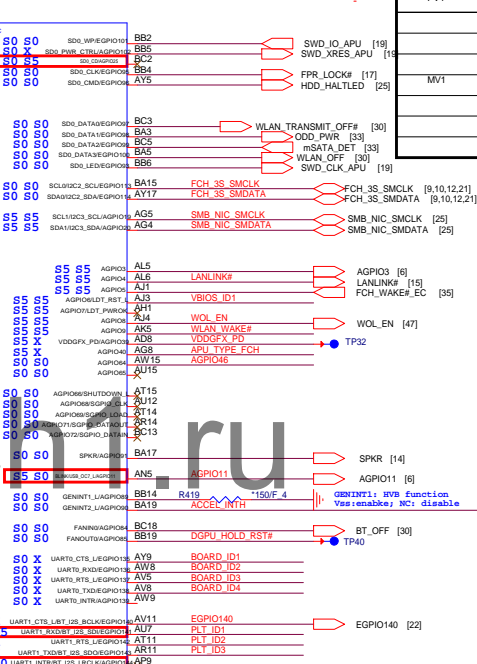


VBIOS_ID	VBIOS_ID1	VBIOS_ID2
Discrete VRAM Group #1	0	0
Discrete VRAM Group #2	0	1
Discrete VRAM Group #3	1	0
UMA	1	1



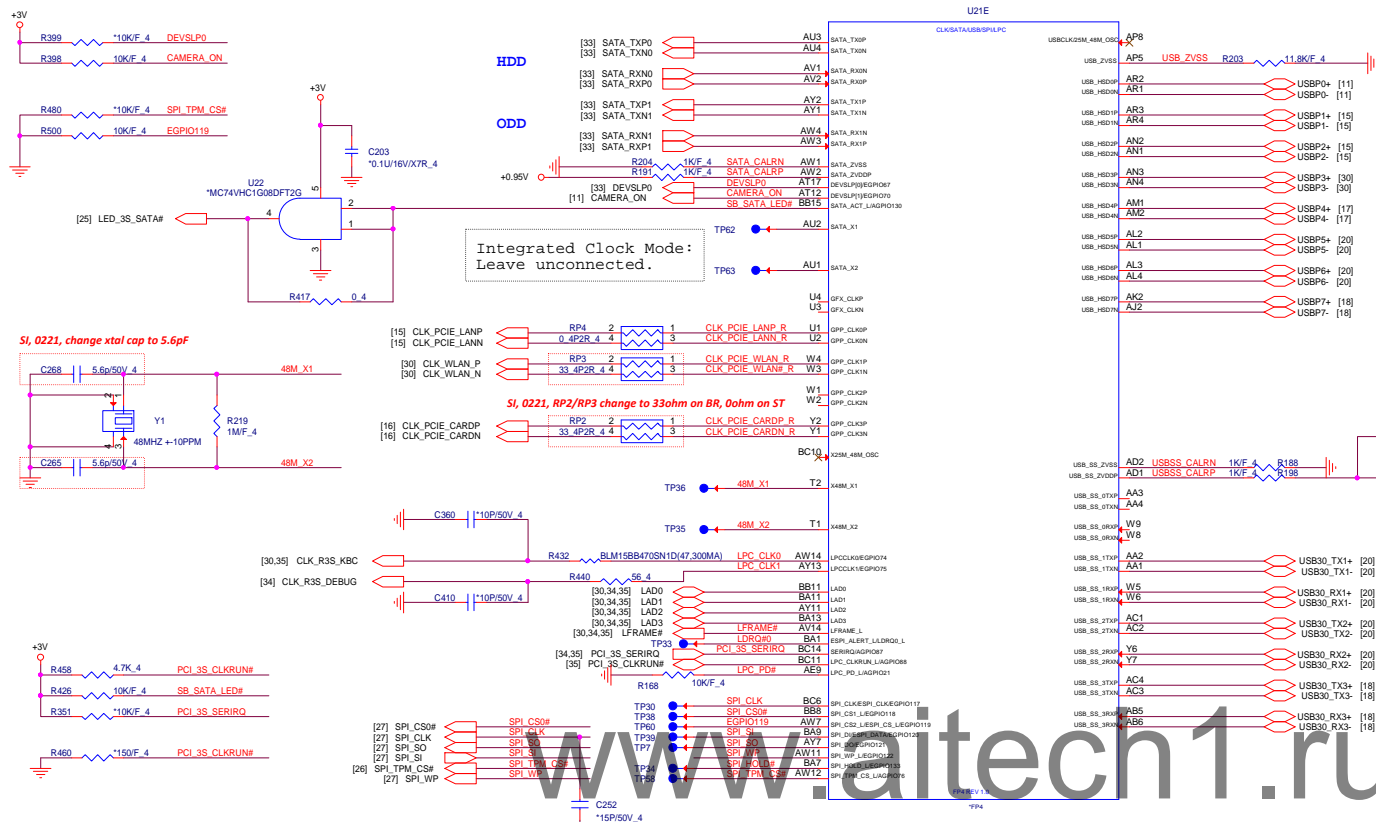
PLT_ID1	PLT_ID2	PLT_ID3
EGPIO141	EGPIO142	EGPIO143
1	0	0

BOARD REVISION	BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4
DB0	0	0	0	0
DB1	0	0	0	1
DB2	0	0	1	0
SI1	0	0	1	1
SIB	0	1	0	1
SI2	0	1	1	0
PV1	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
	1	1	0	0
	1	1	1	1



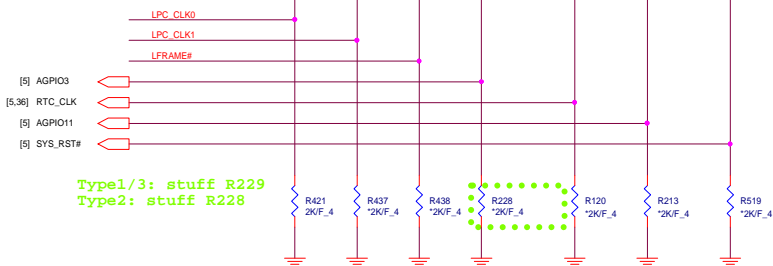
Follow AMD checklist 53537_1_03 suggestion to stuff R118/R120/R122

TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled



STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

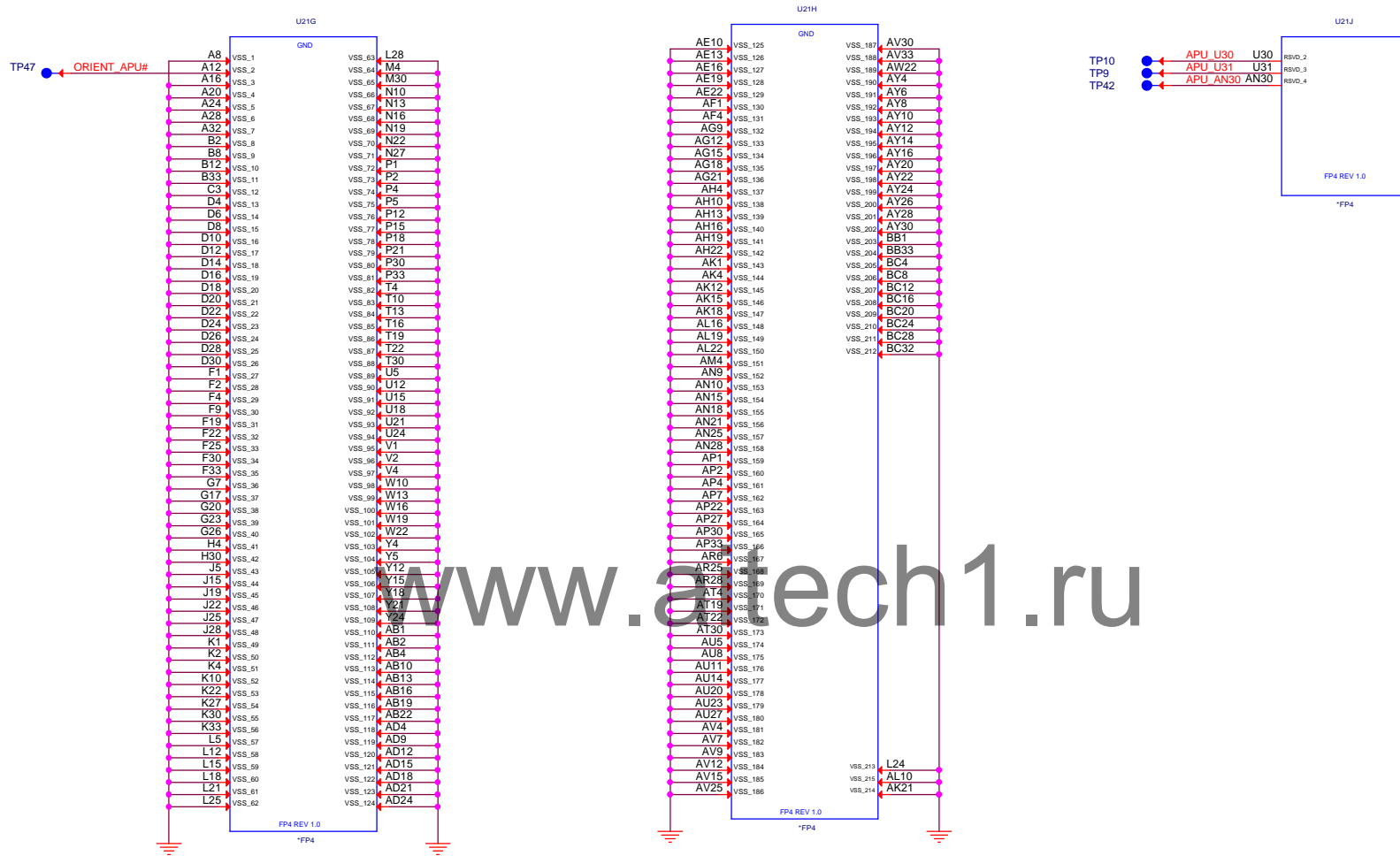
Follow FAE comment: R659 change to 2K, R401 to 10k, R142 is NC

	LPC_CLK0	LPC_CLK1	LFRAME#	AGPIO3 Init Pull-Up	RTC_CLK Init Pull-Up	AGPIO11 Blink Init Pull-Up	SYS_RST# Init Pull-Up
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48MHz crystal clock and generate both internal and external clocks DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM DEFAULT	Coin battery is on board. DEFAULT	LDT_RST#/LDT_PWRGD output to APU DEFAULT	normal reset mode DEFAULT
PULL LOW	BOOT FAIL TIMER DISABLED	Use 100MHz PCIe clock as reference clock and generate internal clocks only	LPC ROM	3.3V SPI ROM DEFAULT	Coin battery is not on board. DEFAULT	LDT_RST#/LDT_PWRGD output to Pads	short reset mode



PROJECT : 400 SERIES
Quanta Computer Inc.

Size Document Number
BR/ST 5/7 (SATA/USB/SPI)
Date: Tuesday, March 01, 2016 Sheet 6 of 53



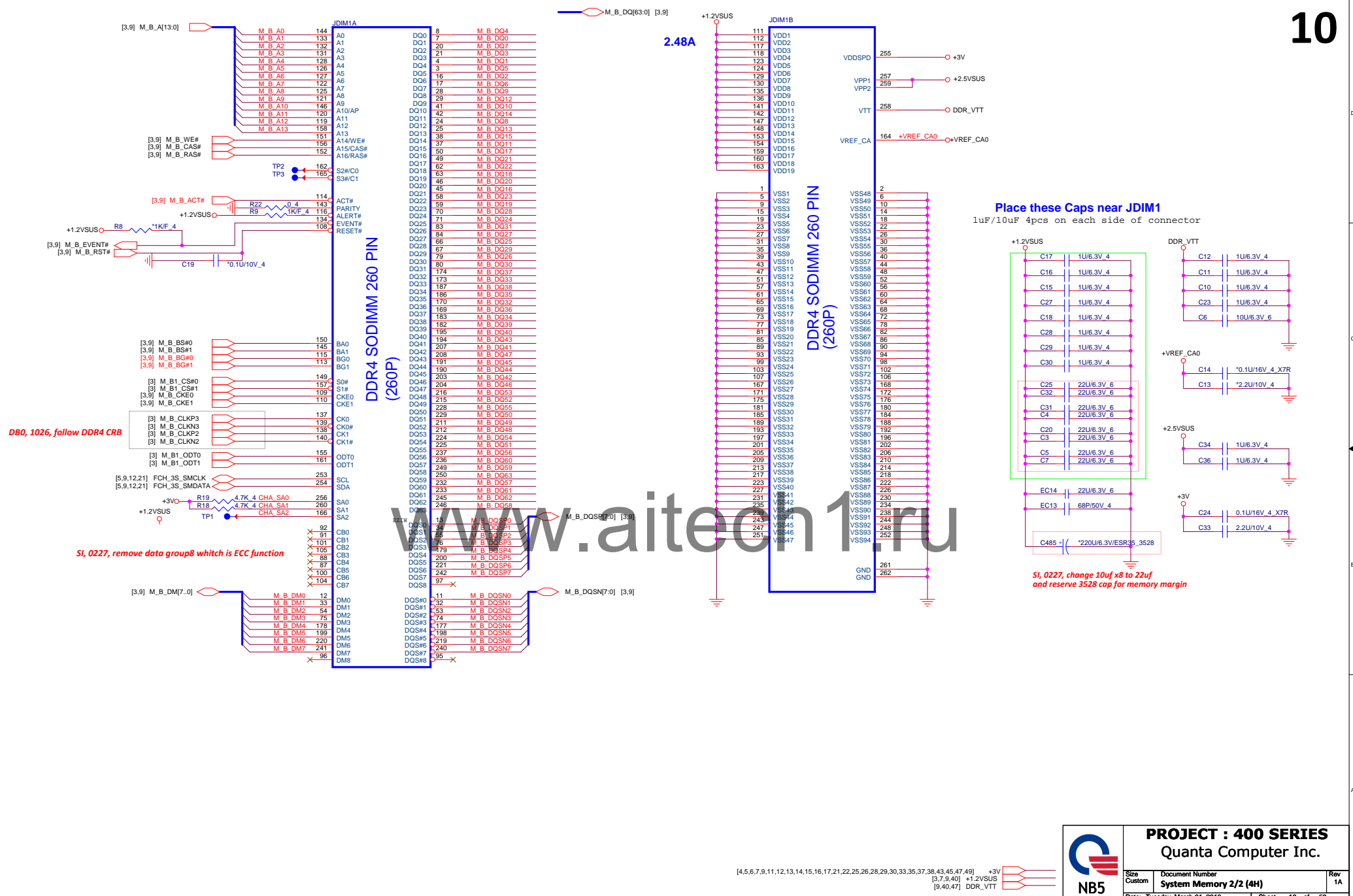
PROJECT : 400 SERIES

Quanta Computer Inc.


Size	Document Number	Rev
	BR/ST 7/7 (GND)	1A

Date: Tuesday, March 01, 2016 Sheet 8 of 53





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PROJECT : 400 SERIES
Quanta Computer Inc.

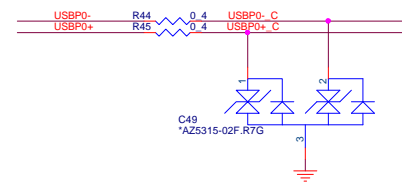
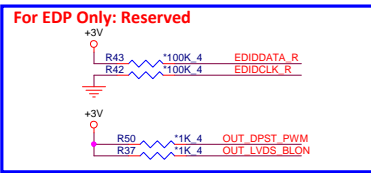
Size Custom	Document Number System Memory 2/2 (4H)	Rev 1A
Date: Tuesday, March 01, 2016	Sheet 10 of 53	

[4,5,6,7,9,11,12,13,14,15,16,17,21,22,25,26,28,29,30,33,35,37,38,43,45,47,49] +3V
[3,7,9,40] +1.2VSUS
[9,40,47] DDR_VTT

LID Switch

11

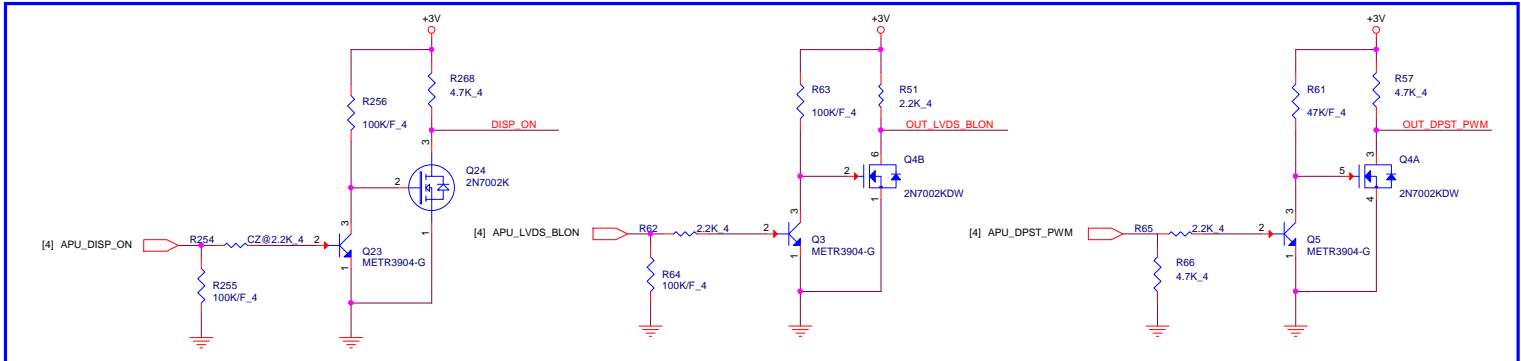
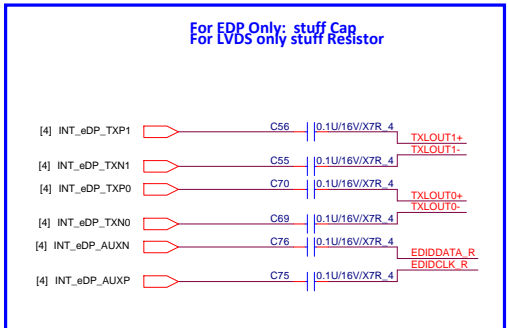
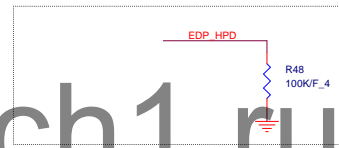
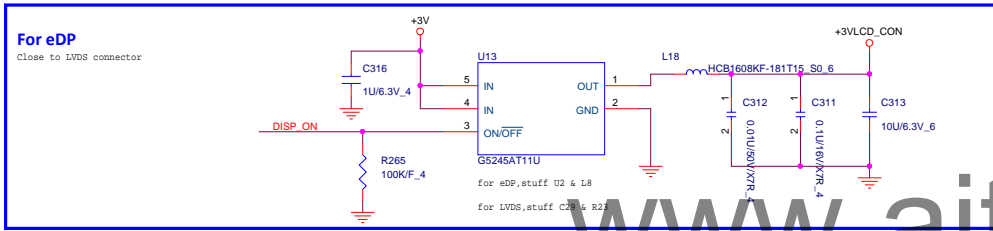
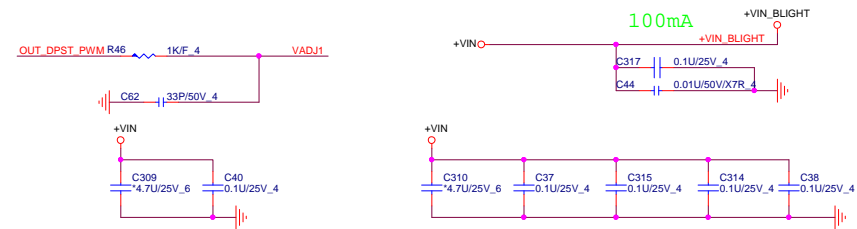
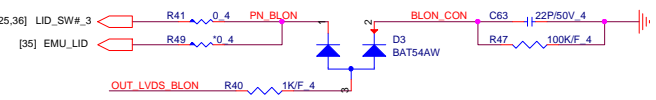
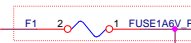
LVDS Conn.



SI, 0220, EMI change solution



SI, 0223, change 0ohm to fuse

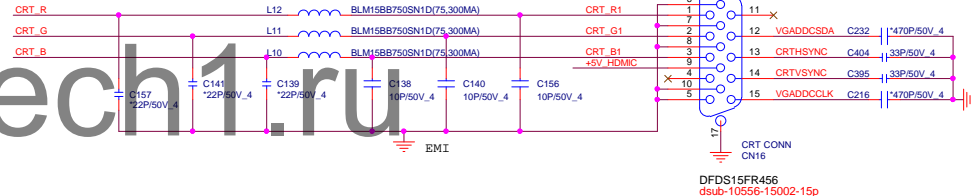


PROJECT : 400 SERIES
Quanta Computer Inc.

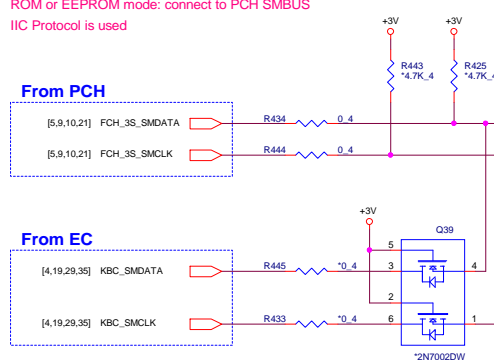
Size Custom Document Number LCD CONN/LID/CAM/D-MIC Rev 1A

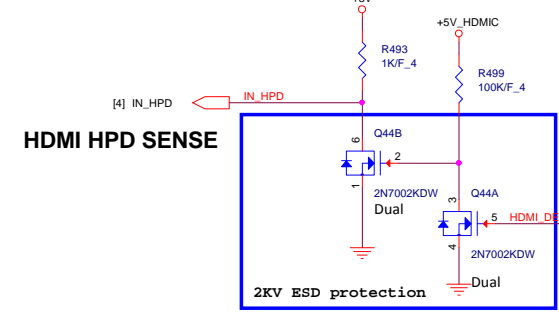
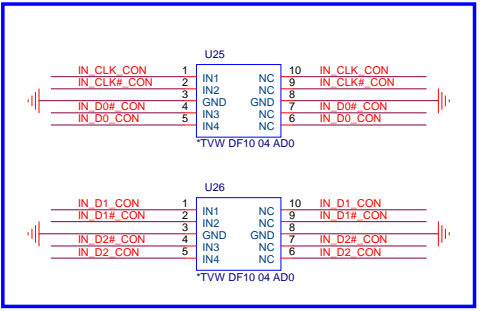
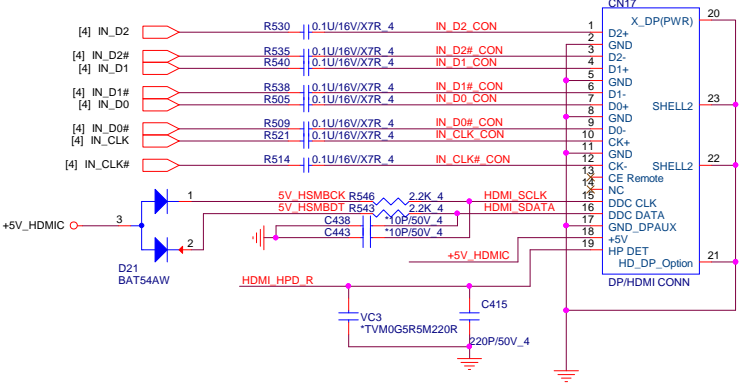
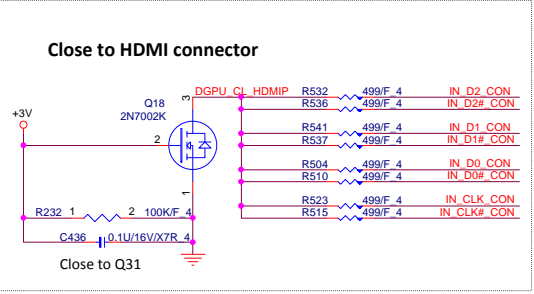
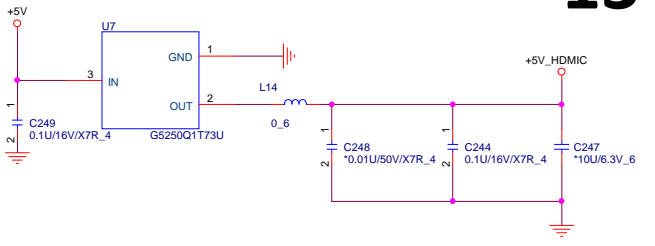
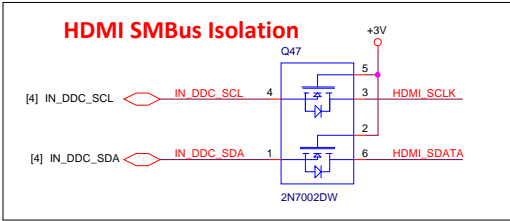
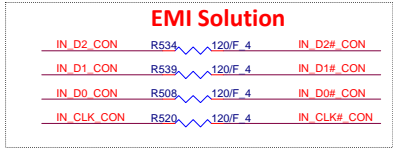
Date: Tuesday, March 01, 2016 Sheet 11 of 53

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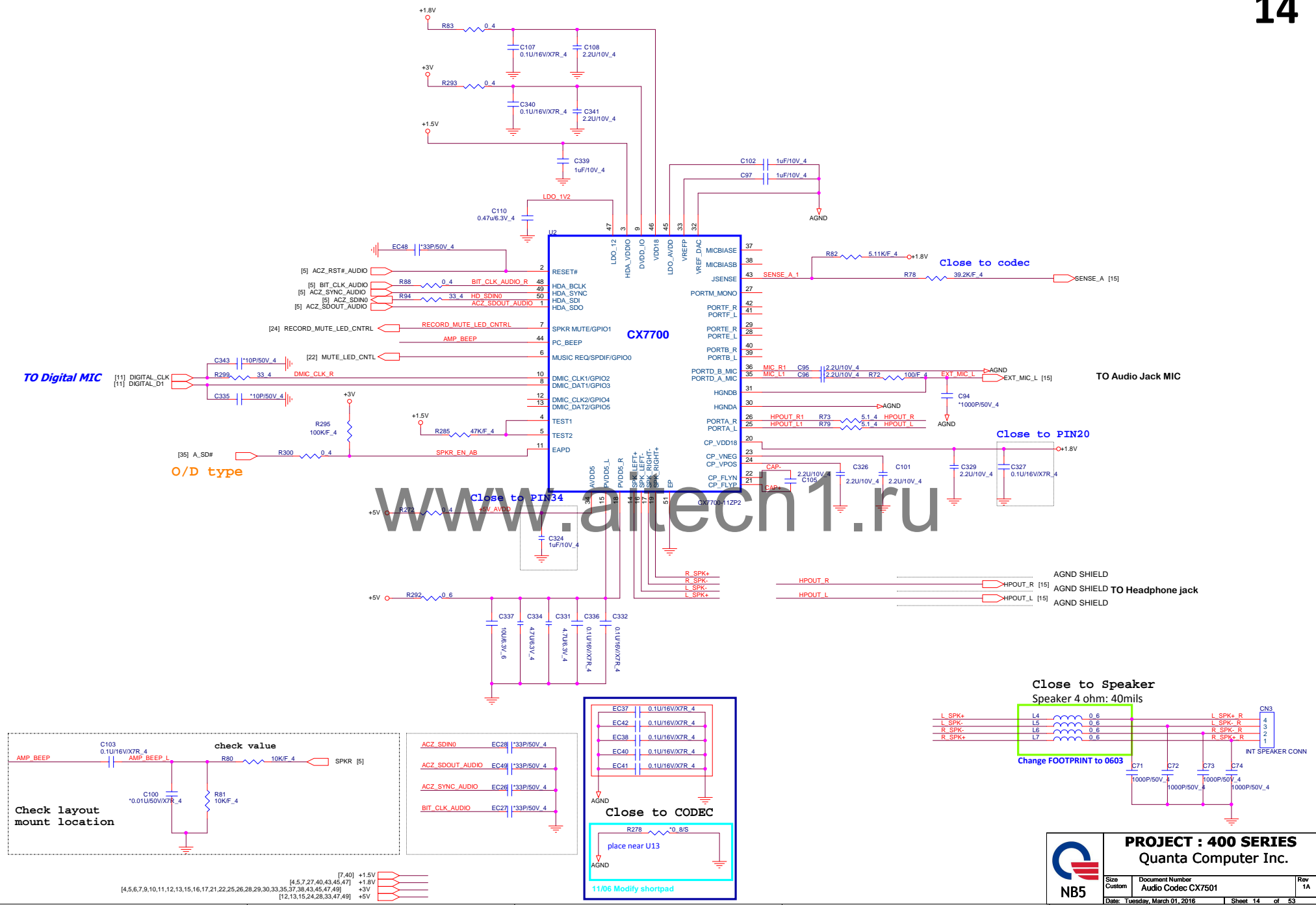


EP mode: Pin2, Pin3 connect to EC SMBUS
ROM or EEPROM mode: connect to PCH SMBUS
IIC Protocol is used

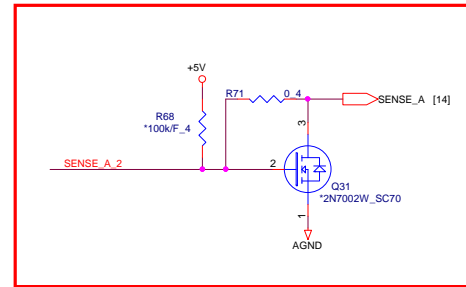
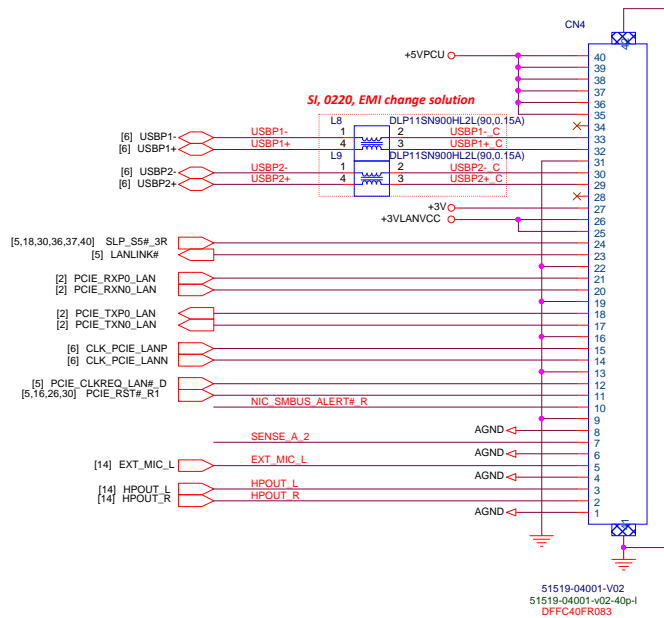




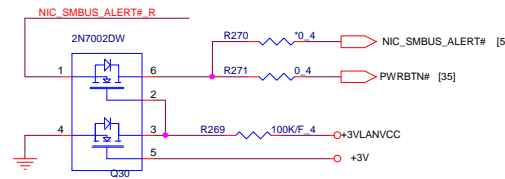
www.aitech1.ru




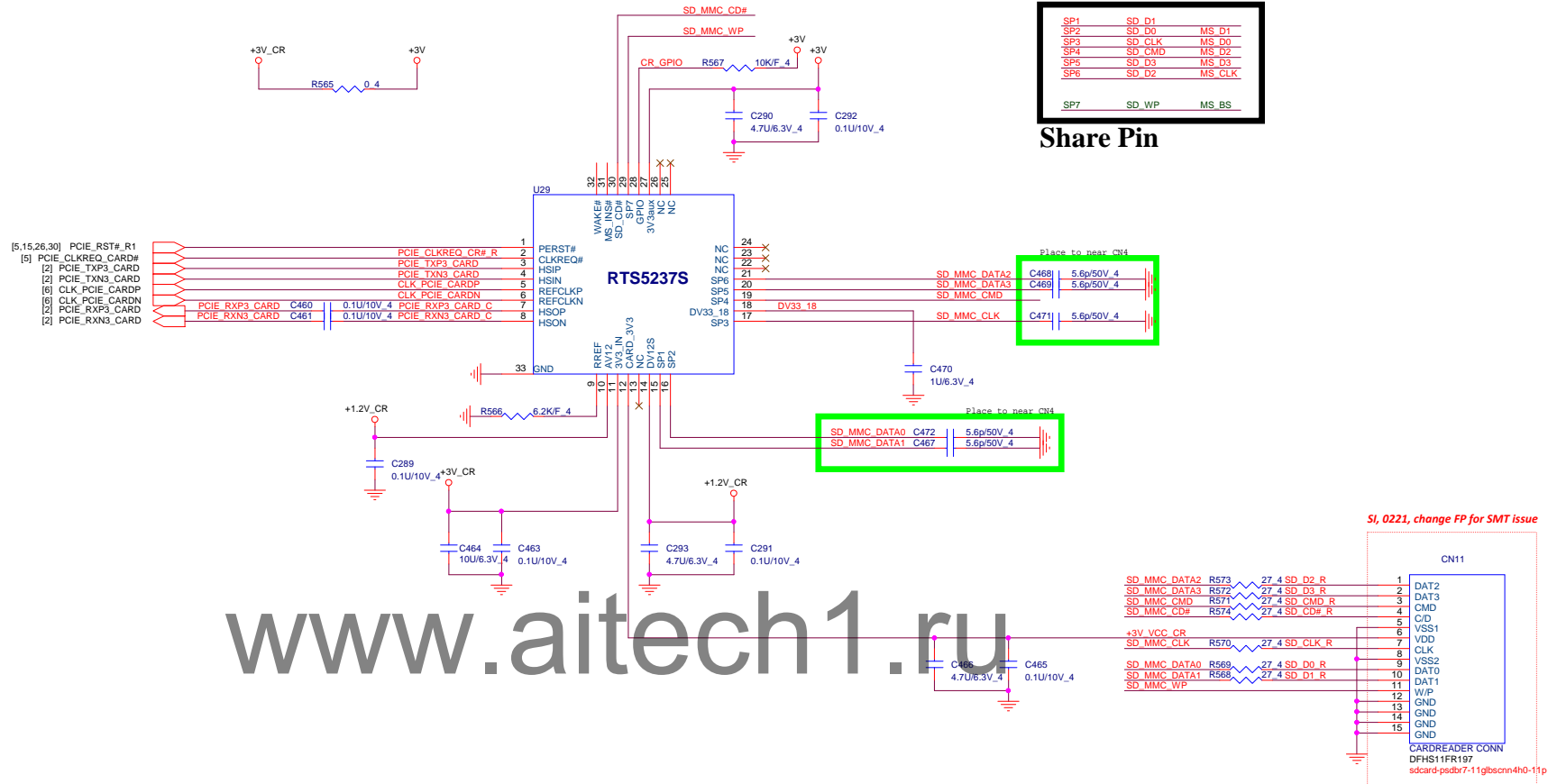
USB2.0 x2/LAN/Headphone_Mic Combo Jack Daughter Board Connector



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		PROJECT : 400 SERIES	
		Quanta Computer Inc.	
Size Custom	Document Number Audio/USB BOARD	Rev 1A	
Date: Tuesday, March 01, 2016	Sheet 15 of 53		

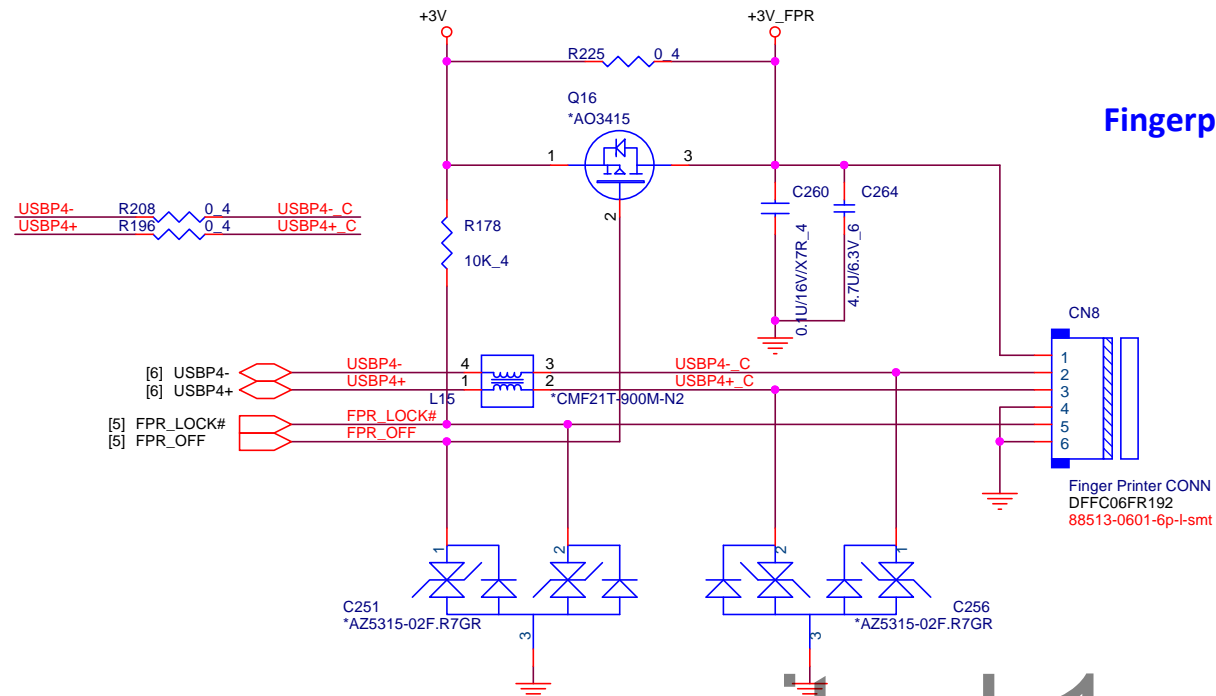


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PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CARD READER	1A
Date: Tuesday, March 01, 2016	Sheet 16 of 53	



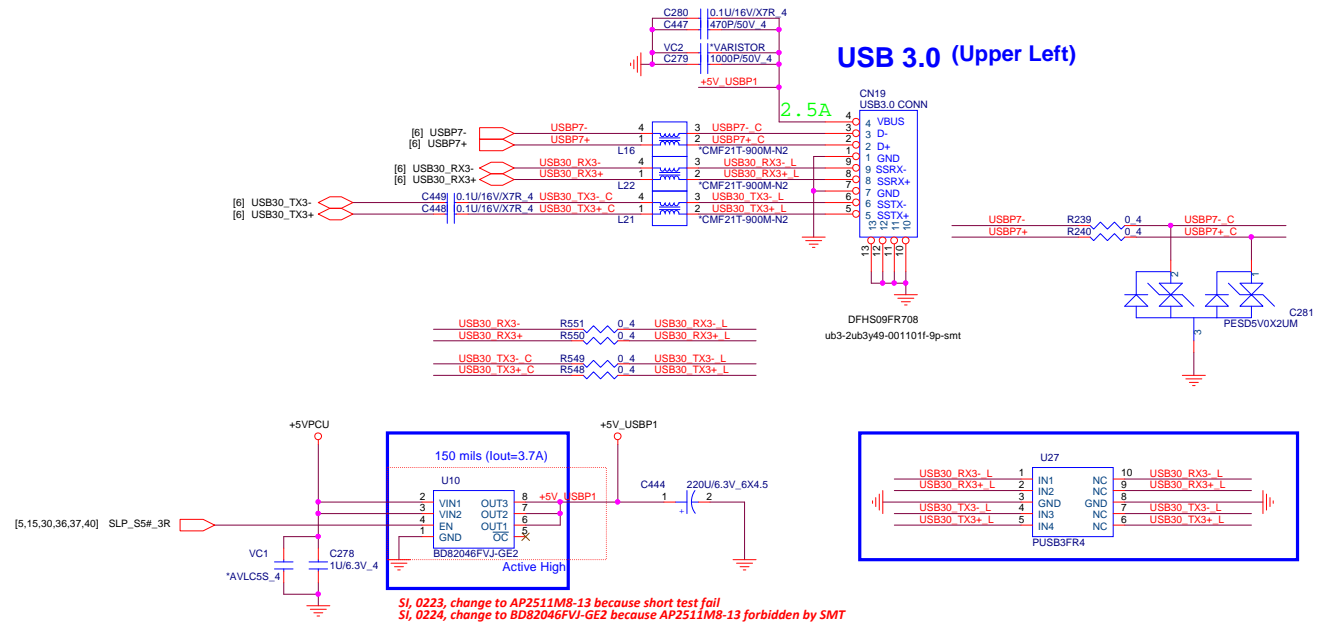
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PROJECT : 400 SERIES
Quanta Computer Inc.


Size Custom	Document Number Finger Printer	Rev 1A
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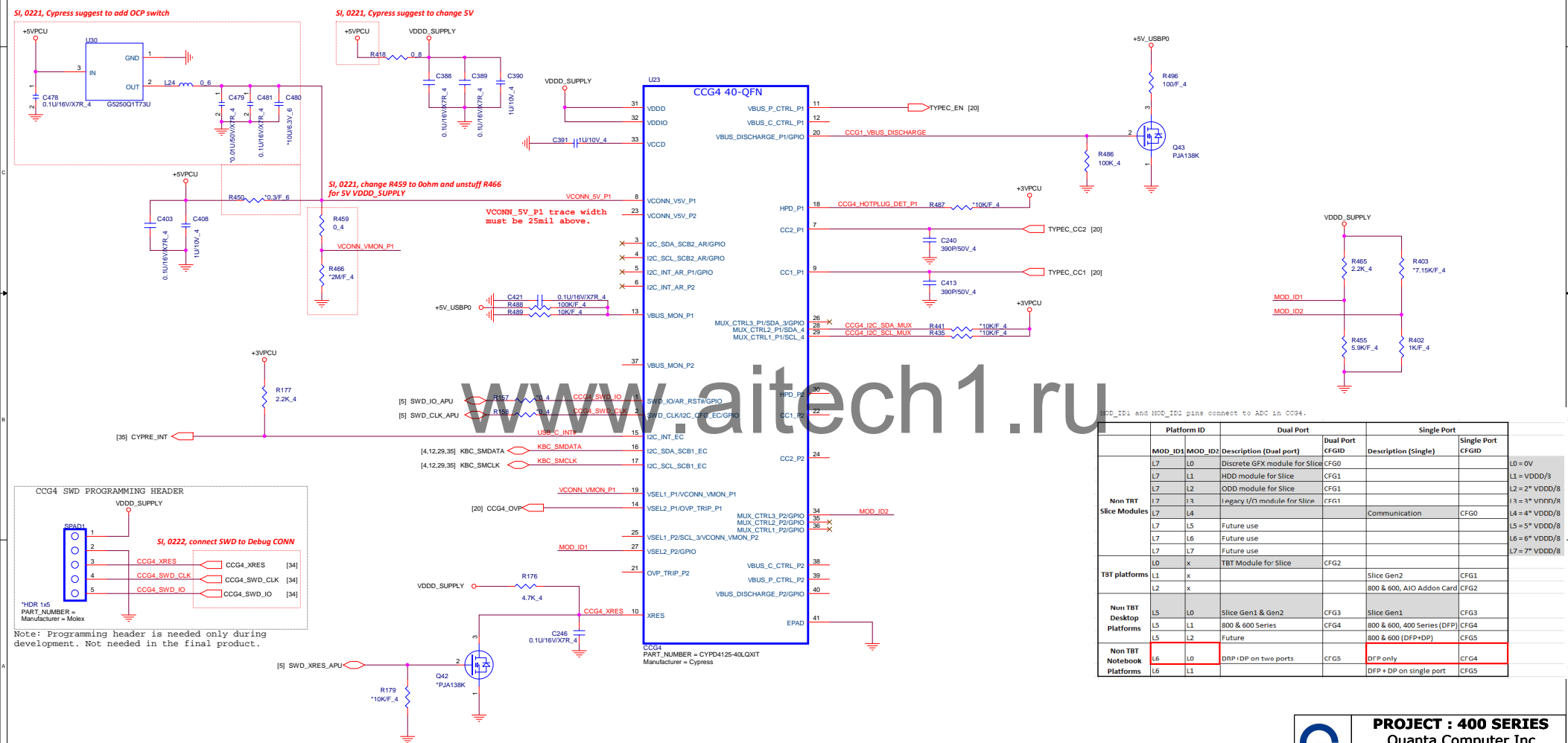
Date: Tuesday, March 01, 2016 Sheet 17 of 53



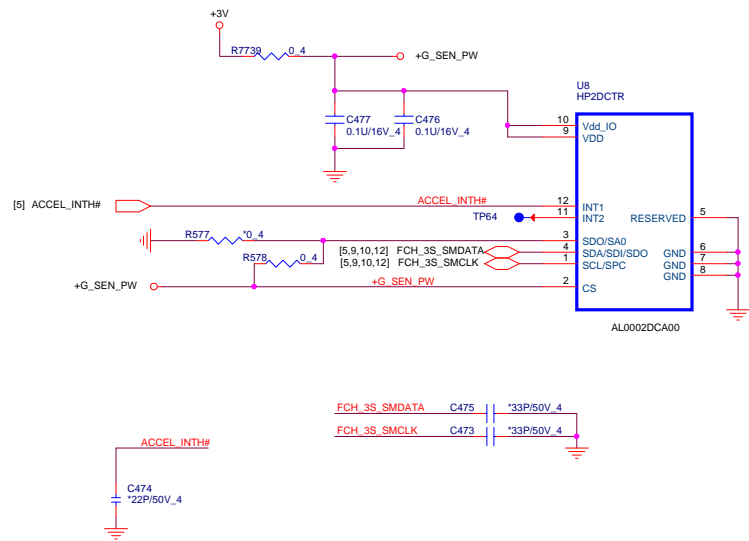
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[15,19,20,38,39,40,41,42,43,45,47,49] +5VPCU
[7,19,22,23,24,27,28,29,34,35,36,37,38,39,40,42,47,48] +3VPCU

	PROJECT : 400 SERIES		
	Quanta Computer Inc.		
	Size Custom	Document Number USB 3.0/USB3 Re-driver	Rev 1A
	Date: Tuesday, March 01, 2016	Sheet 18 of 53	




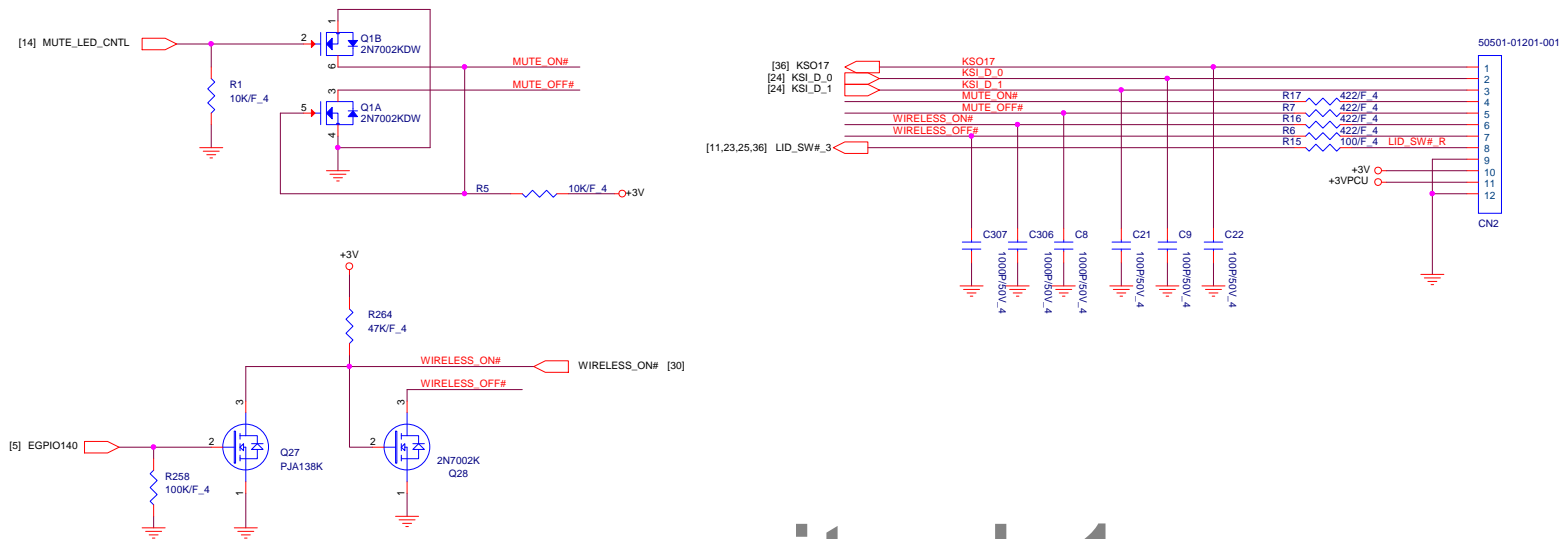
Accelerometer Sensor



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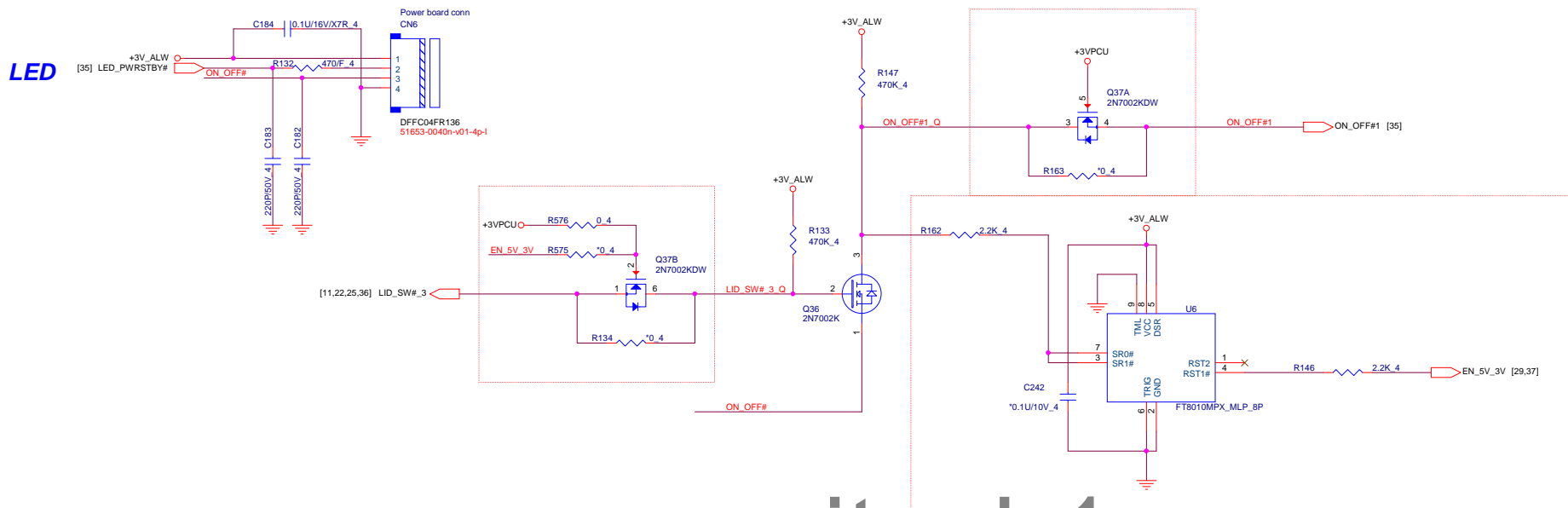
[7, 19, 22, 23, 24, 27, 28, 29, 34, 35, 36, 37, 38, 39, 40, 42, 47, 48] [15, 18, 19, 20, 38, 39, 40, 41, 42, 43, 45, 47, 49] +5VPCU
+3VPCU

 PROJECT : 400 SERIES Quanta Computer Inc.		Size	Document Number	Rev
		Custom	Accelerometer	1A
Date:	Tuesday, March 01, 2016	Sheet	21 of	53




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Power Button Connector

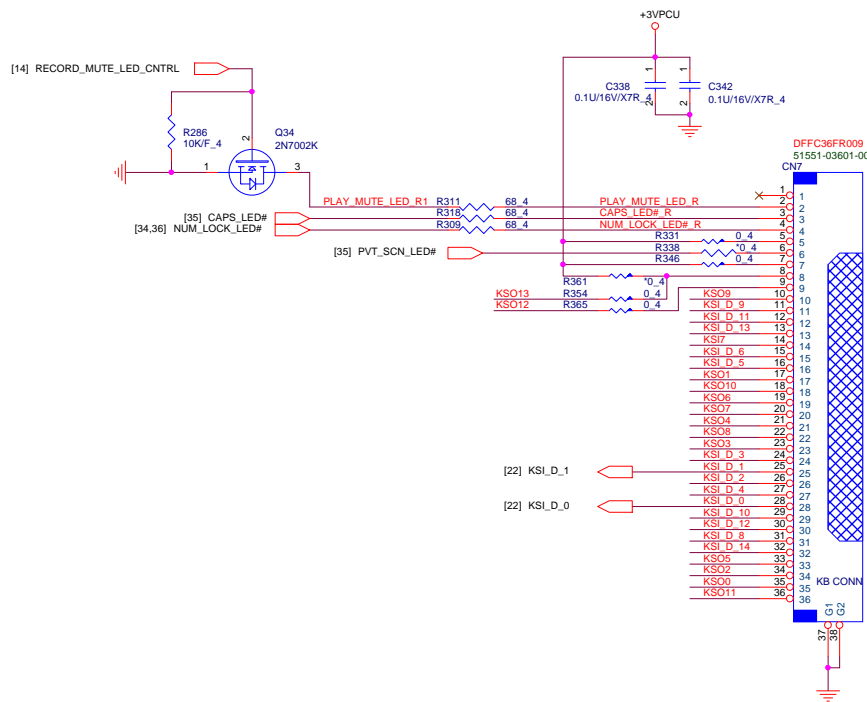


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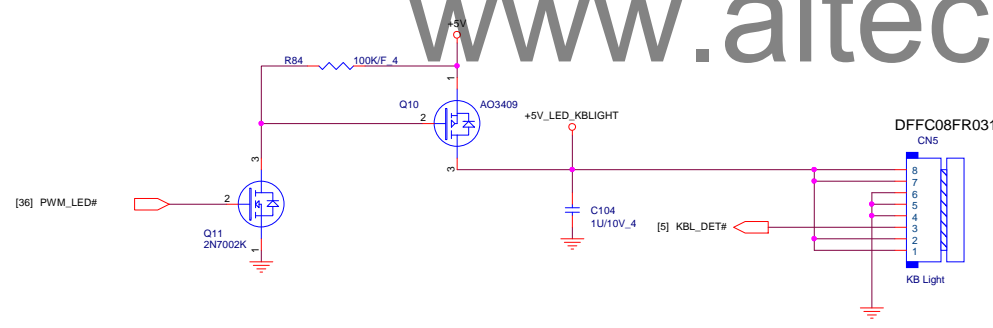
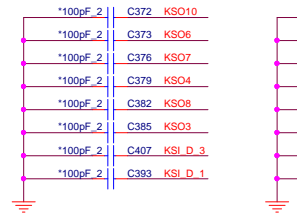
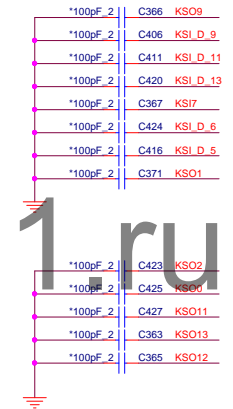
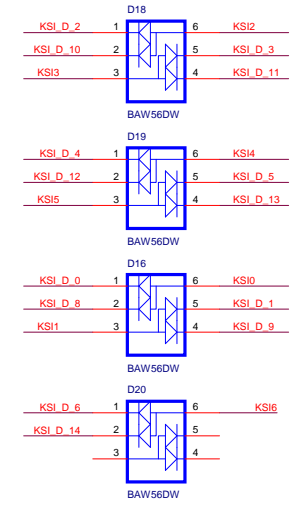
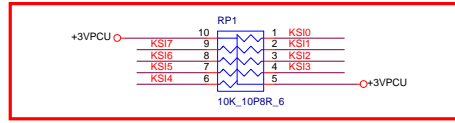
[37,38,39,48] +3V_ALW
[4,5,6,7,9,10,11,12,13,14,15,16,17,21,22,25,26,28,29,30,33,35,37,38,43,45,47,49] +3V
[12,13,14,15,24,28,33,47,49] +5V
[7,19,22,24,27,28,29,34,35,36,37,38,39,40,42,47,48] +3VPCU

 PROJECT : 400 SERIES Quanta Computer Inc.		Size Custom	Document Number 33 -- PB/LID	Rev 1A
		Date: Tuesday, March 01, 2016	Sheet 23 of 53	

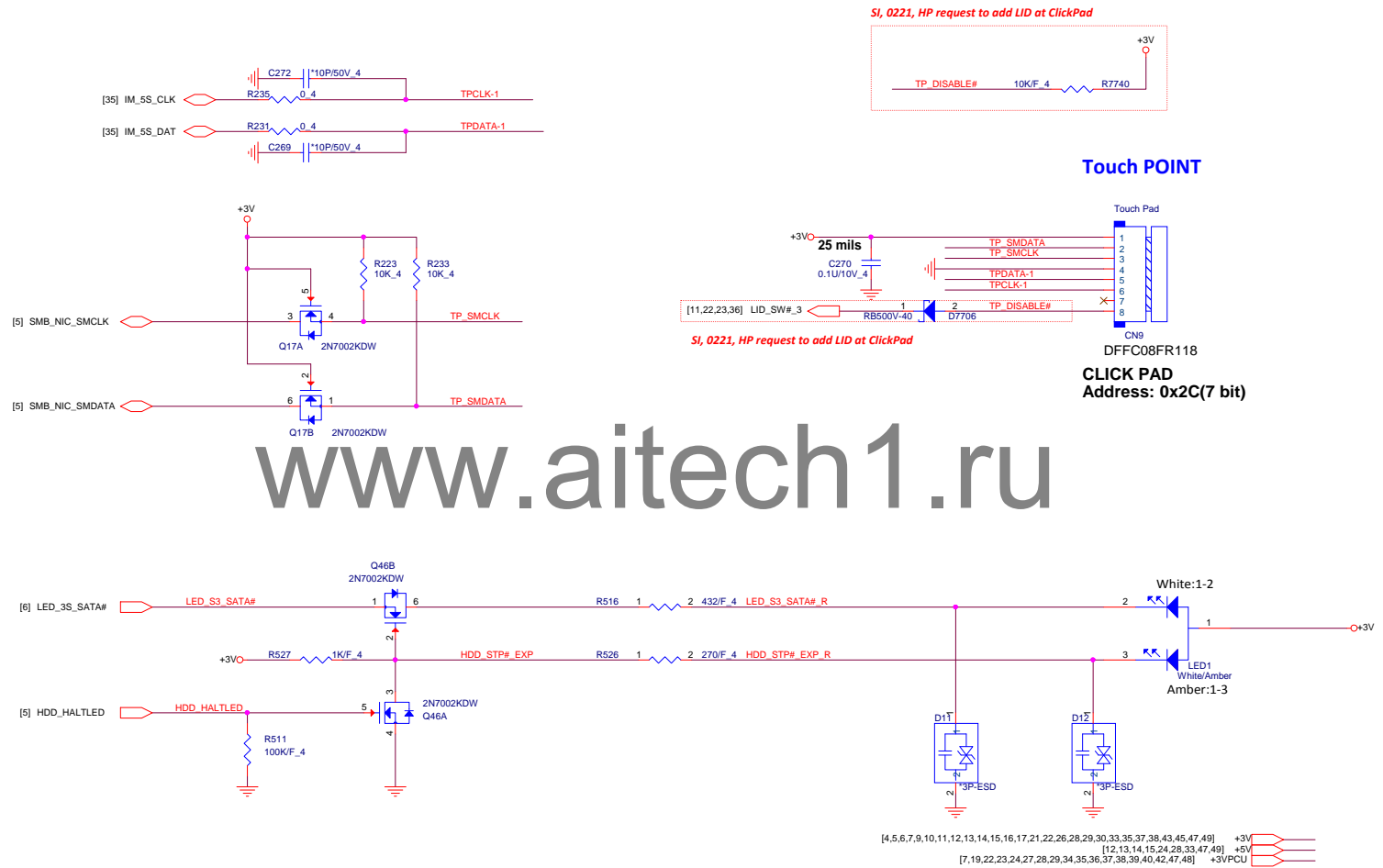
KEYBOARD Con.



KEYBOARD PULL-UP



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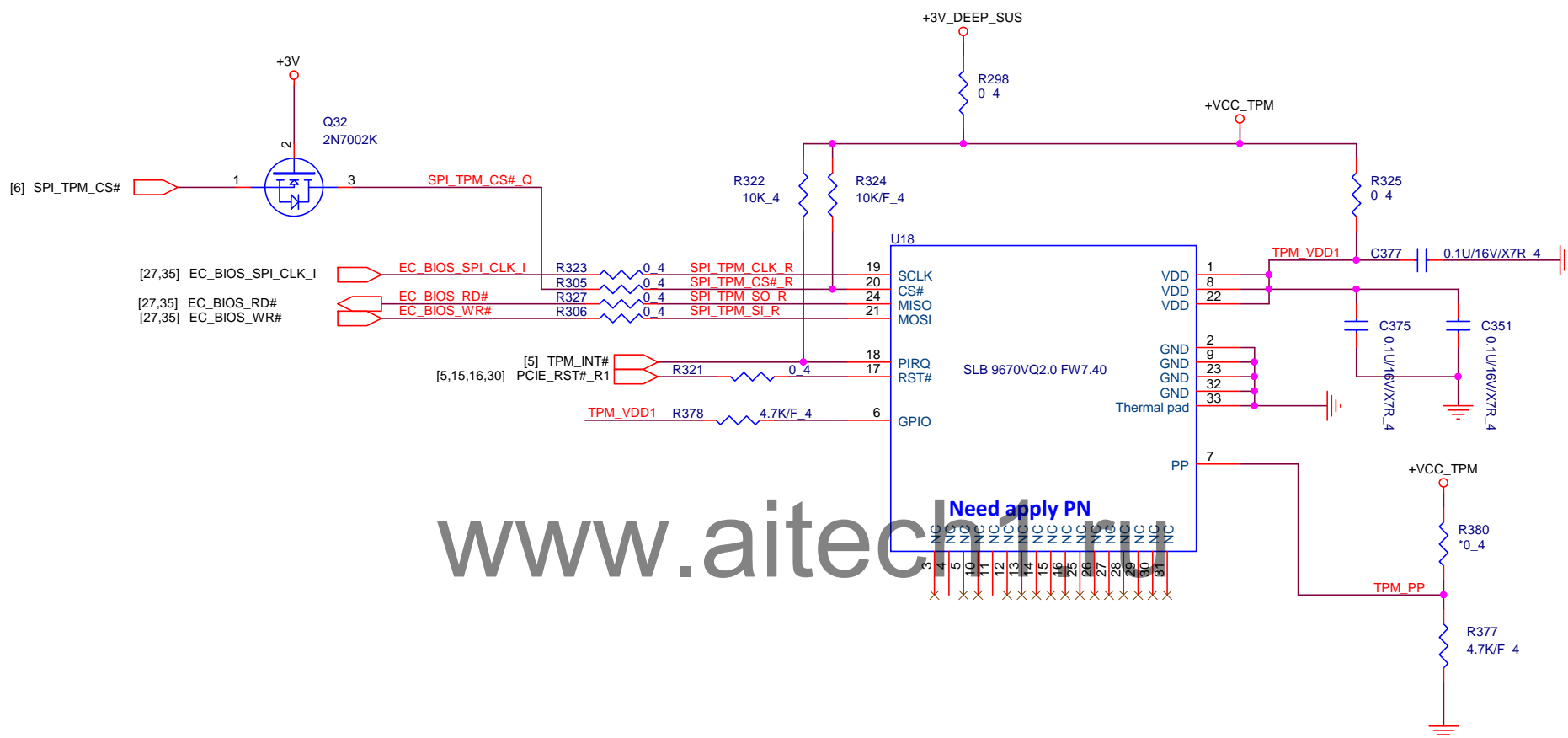


PROJECT : 400 SERIES
Quanta Computer Inc.

Size	Document Number	Rev
Custom	34 -- Forced Pad/Card reader	1A
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TPM (1.2 or 2.0)

26



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PROJECT : 400 SERIES
Quanta Computer Inc.

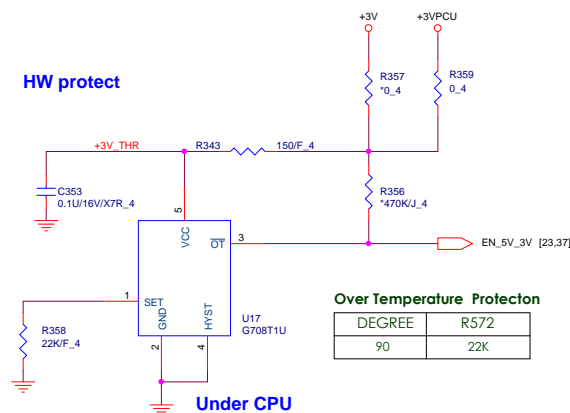
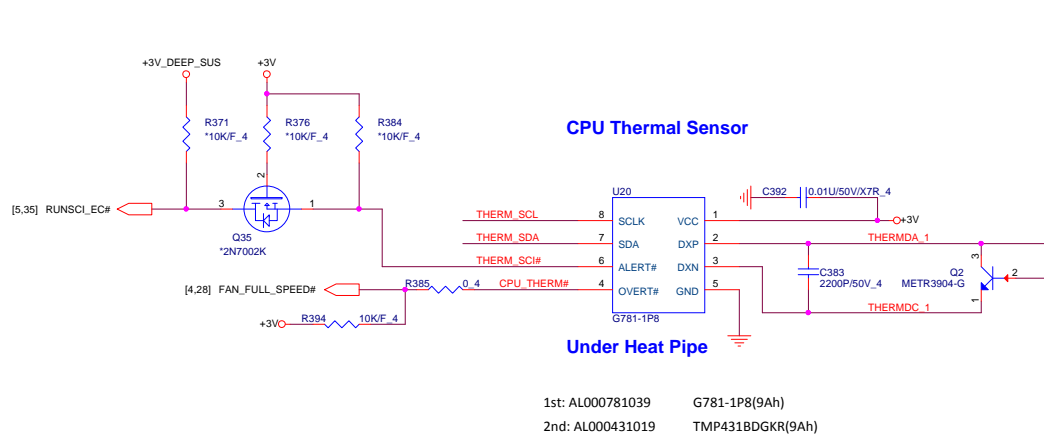
Size Custom	Document Number TPM SLB9665_QFN	Rev 1A
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Date: Tuesday, March 01, 2016 Sheet 26 of 53

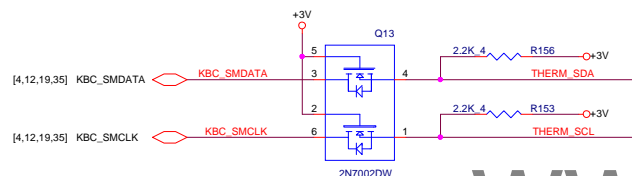


2

1



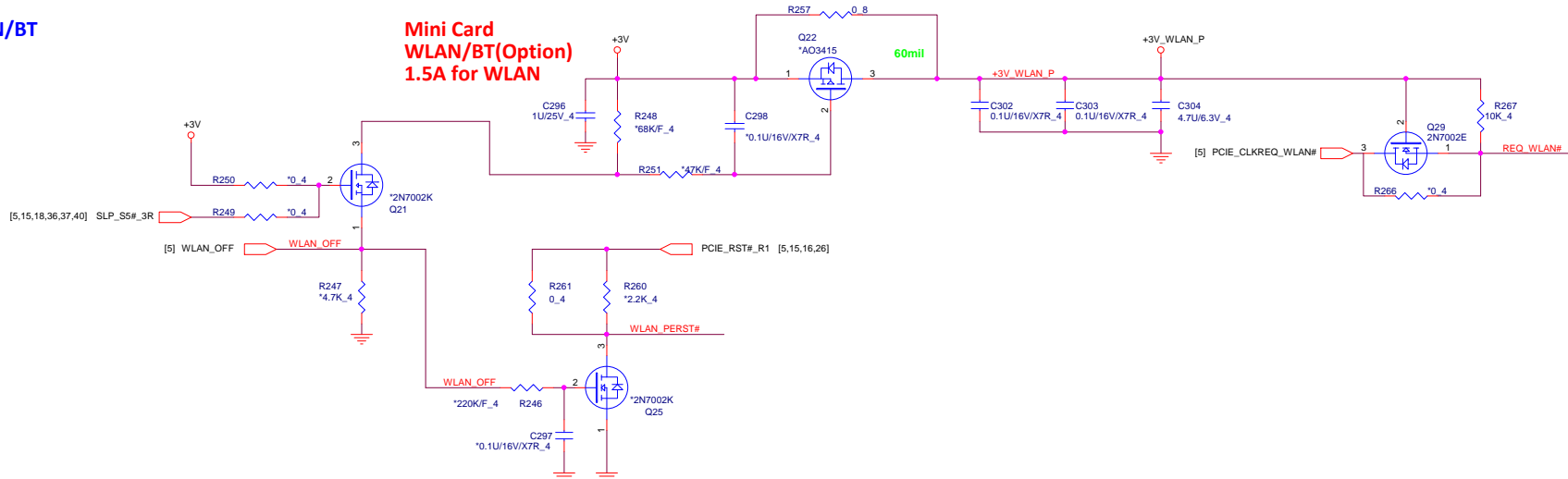
$$RSET \text{ (K OHM)} = 0.0012T^2 - 0.9308T + 96.147$$



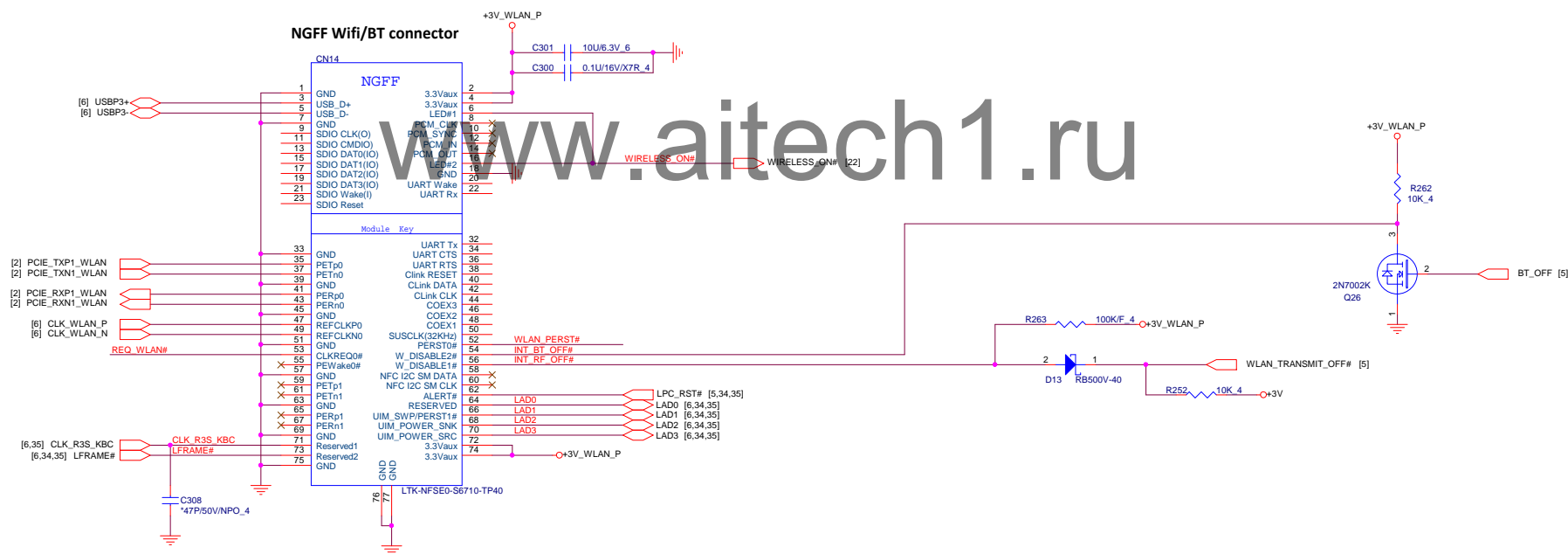
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[4,5,6,7,9,10,11,12,13,14,15,16,17,21,22,25,26,28,30,33,35,37,38,43,45,47,49] +3V
[7,19,22,23,24,27,28,34,35,36,37,38,39,40,42,47,48] +3VPCU

Mini Card WLAN/BT(Optional) 1.5A for WLAN



NGFF Wifi/BT connector



[4,5,6,7,9,10,11,12,13,14,15,16,17,21,22,25,26,28,29,33,35,37,38,43,45,47,49] +3V
[12,13,14,15,24,28,33,47,49] +5V
[7,19,22,23,24,27,28,29,34,35,36,37,38,39,40,42,47,48] +3VPCU




PROJECT : 400 SERIES
Quanta Computer Inc.

Size Custom Document Number
NGFF WLAN/BT
Date: Tuesday, March 01, 2016 Sheet 30 of 53

Rev 1A

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 NB5	PROJECT : 400 SERIES Quanta Computer Inc.		
	Size Custom	Document Number 38 -- WWAN NGFF/ SSD	Rev 1A
	Date: Tuesday, March 01, 2016	Sheet	31 of 53

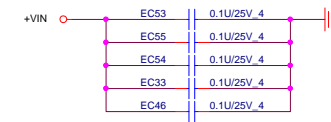
EMI PAD



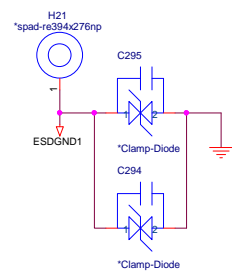
CPU BKT



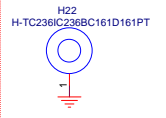
EMI



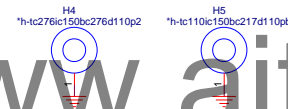
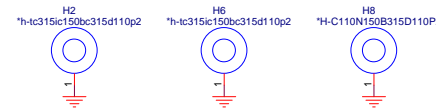
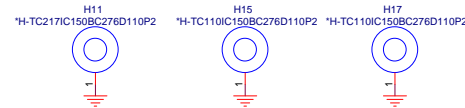
ESD PAD



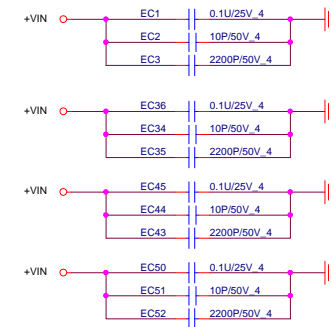
WLAN NUT



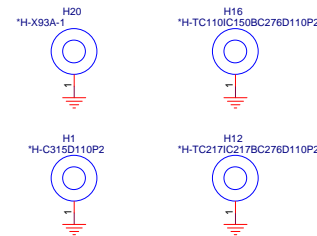
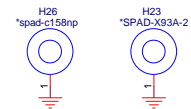
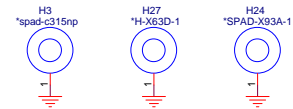
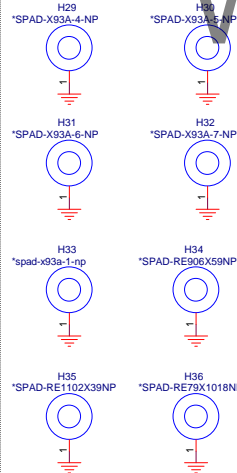
USBC



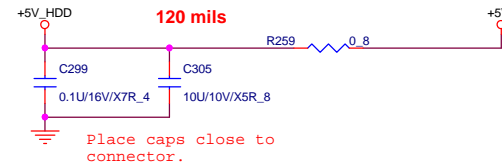
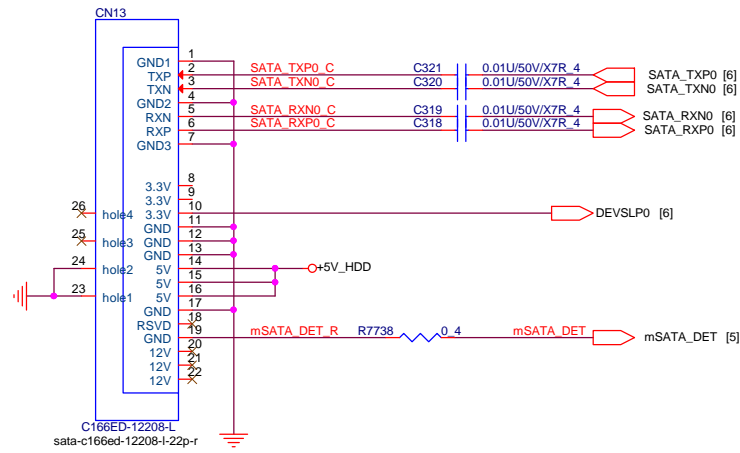
RF



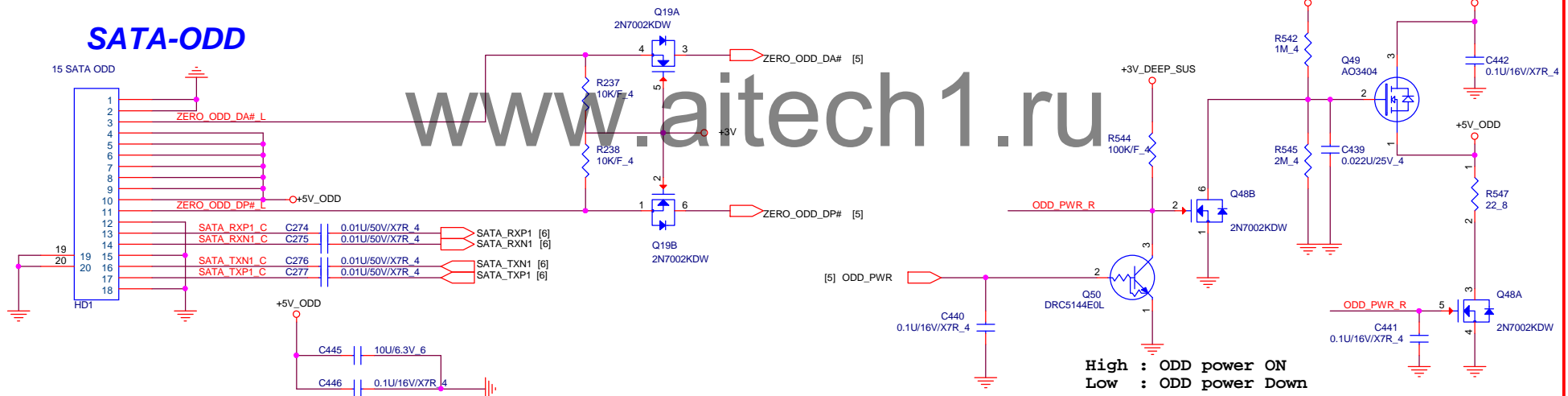
SPAD



SATA-HDD



SATA-ODD



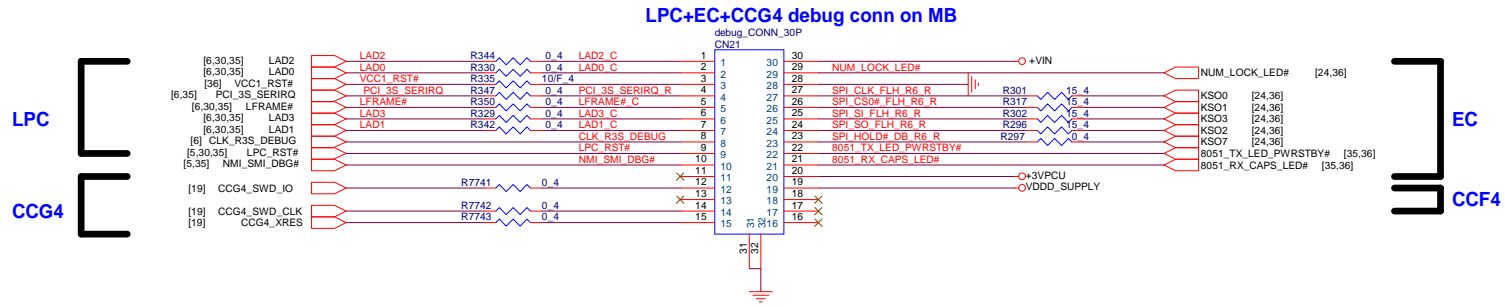
High : ODD power ON
Low : ODD power Down

[4,5,6,7,9,10,11,12,13,14,15,16,17,21,22,25,26,28,29,30,35,37,38,43,45,47,49] +3V
[12,13,14,15,24,28,47,49] +5V
[7,19,22,23,24,27,28,29,34,35,36,37,38,39,40,42,47,48] +3VPCU

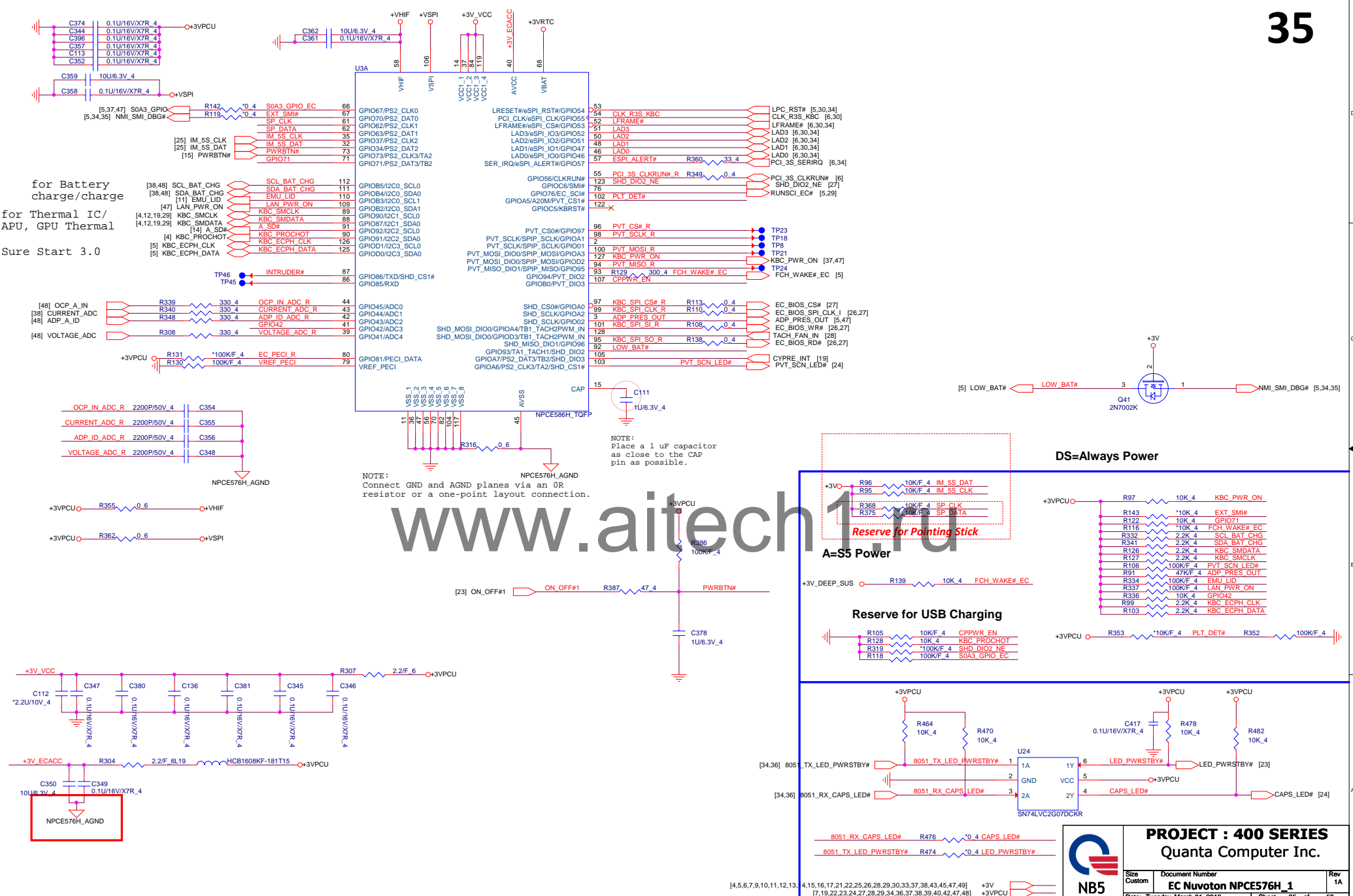


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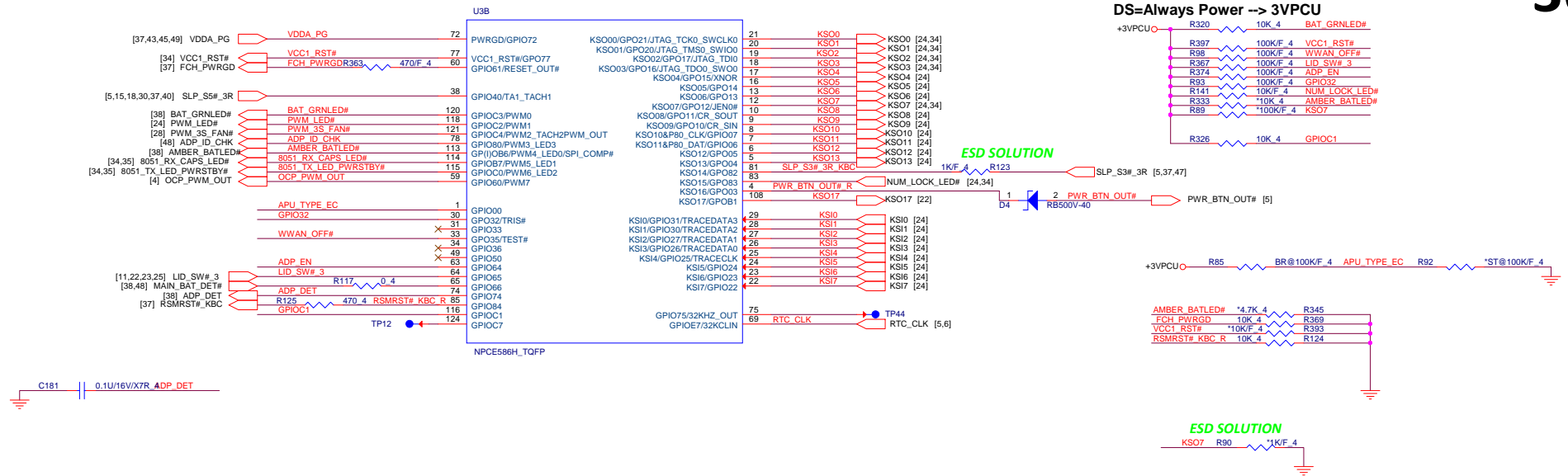
Size B	Document Number 37 -- HDD/ODD	Rev 1A
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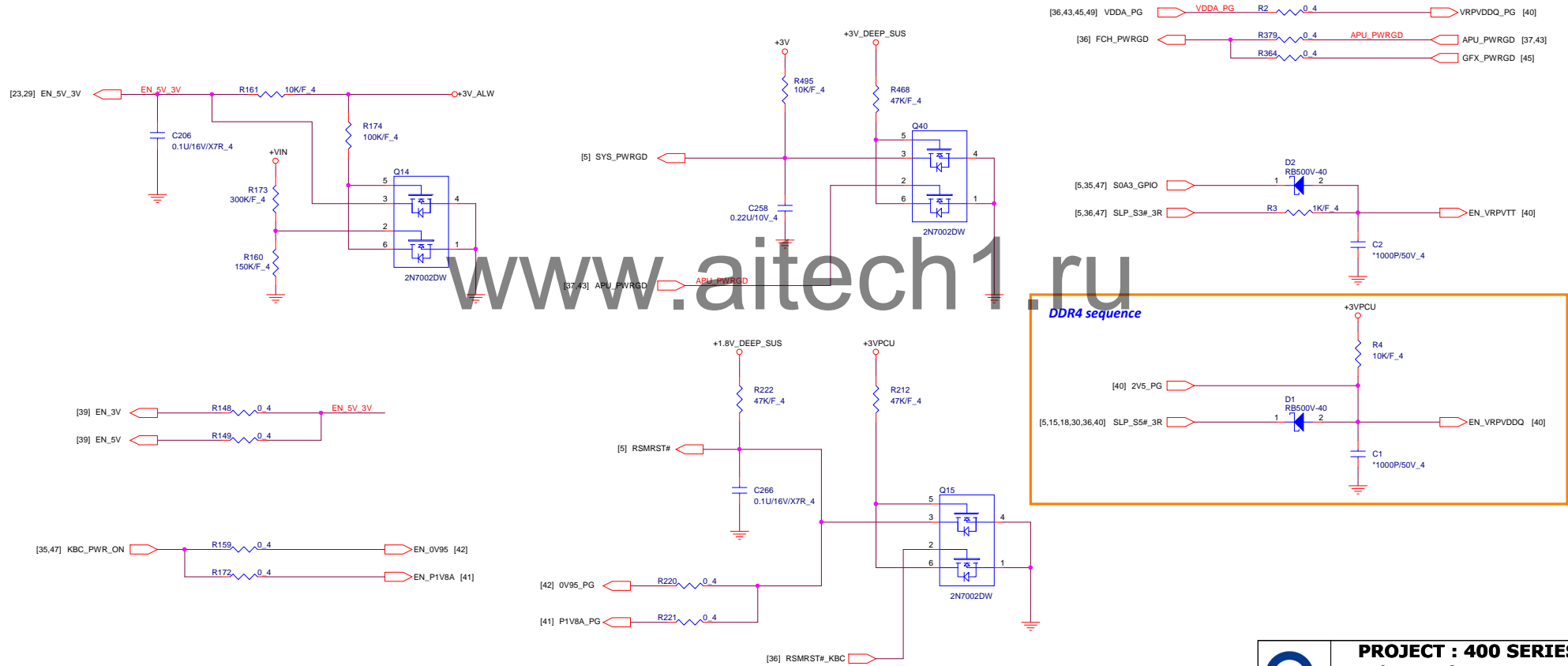
www.aitech1.ru

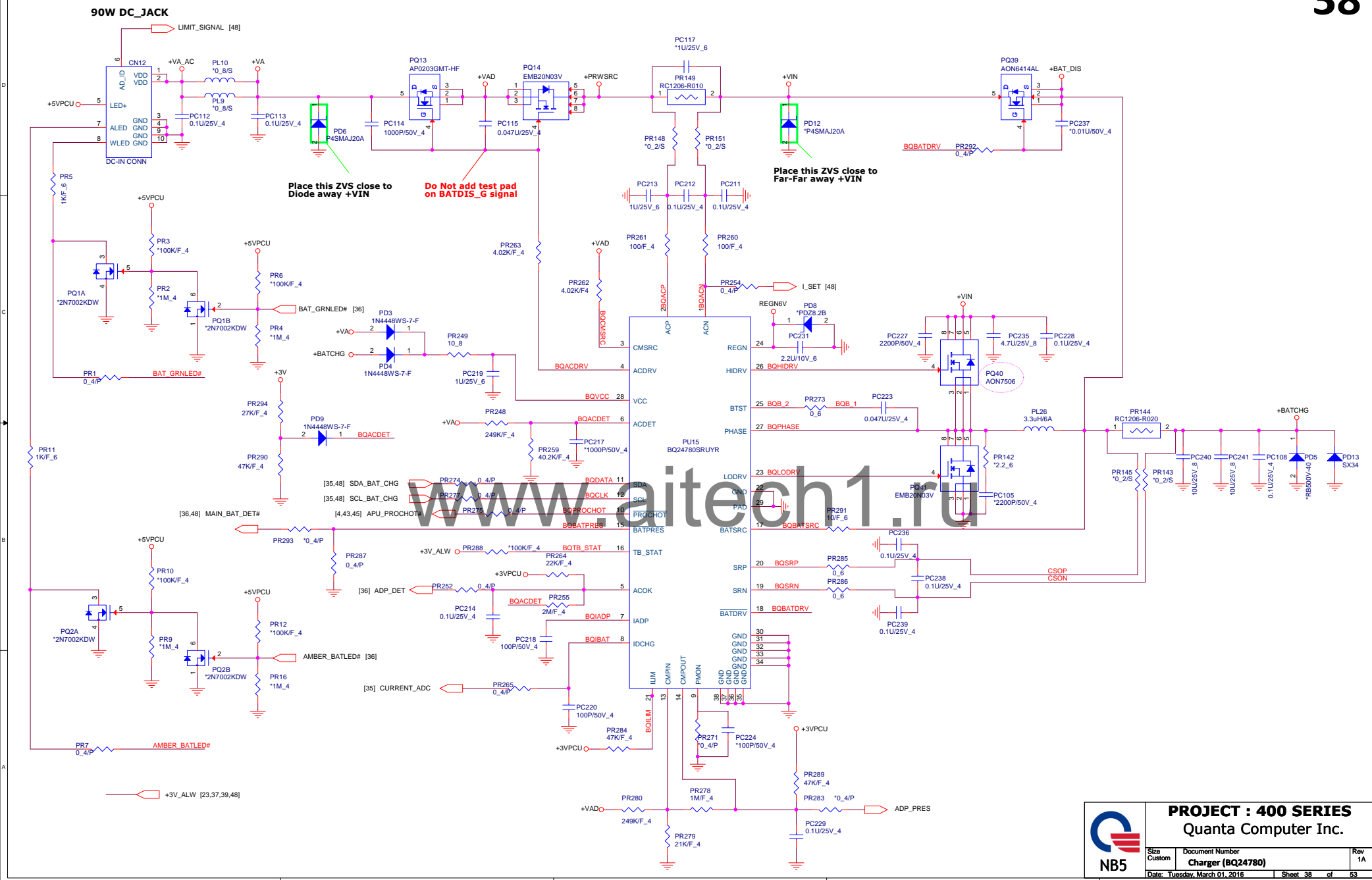


[4,5,6,7,9,10,11,12,13, 4,15,16,17,21,22,25,26,28,29,30,33,37,38,43,45,47,49] +3V
[7,19,22,23,24,27,28,29,34,36,37,38,39,40,42,47,48] +3VPCU



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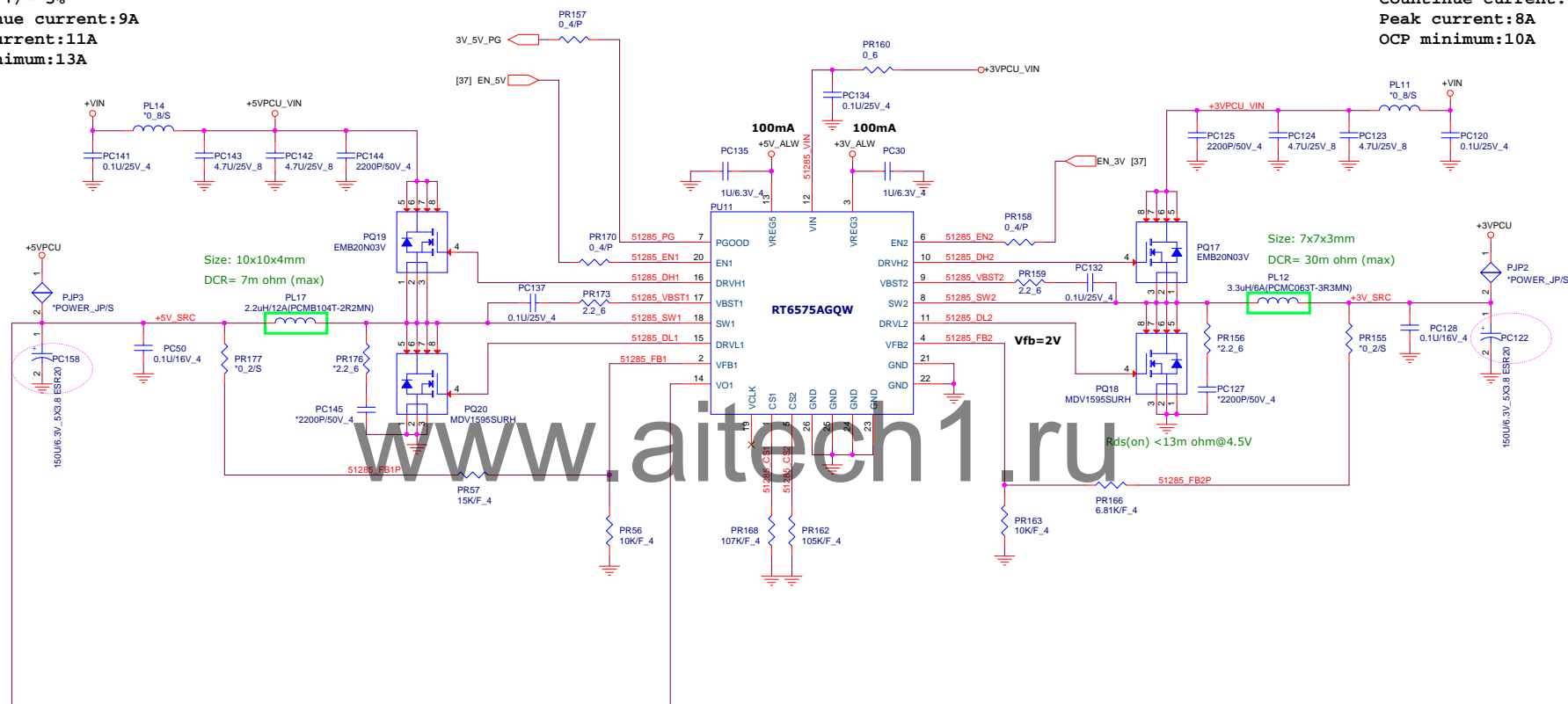


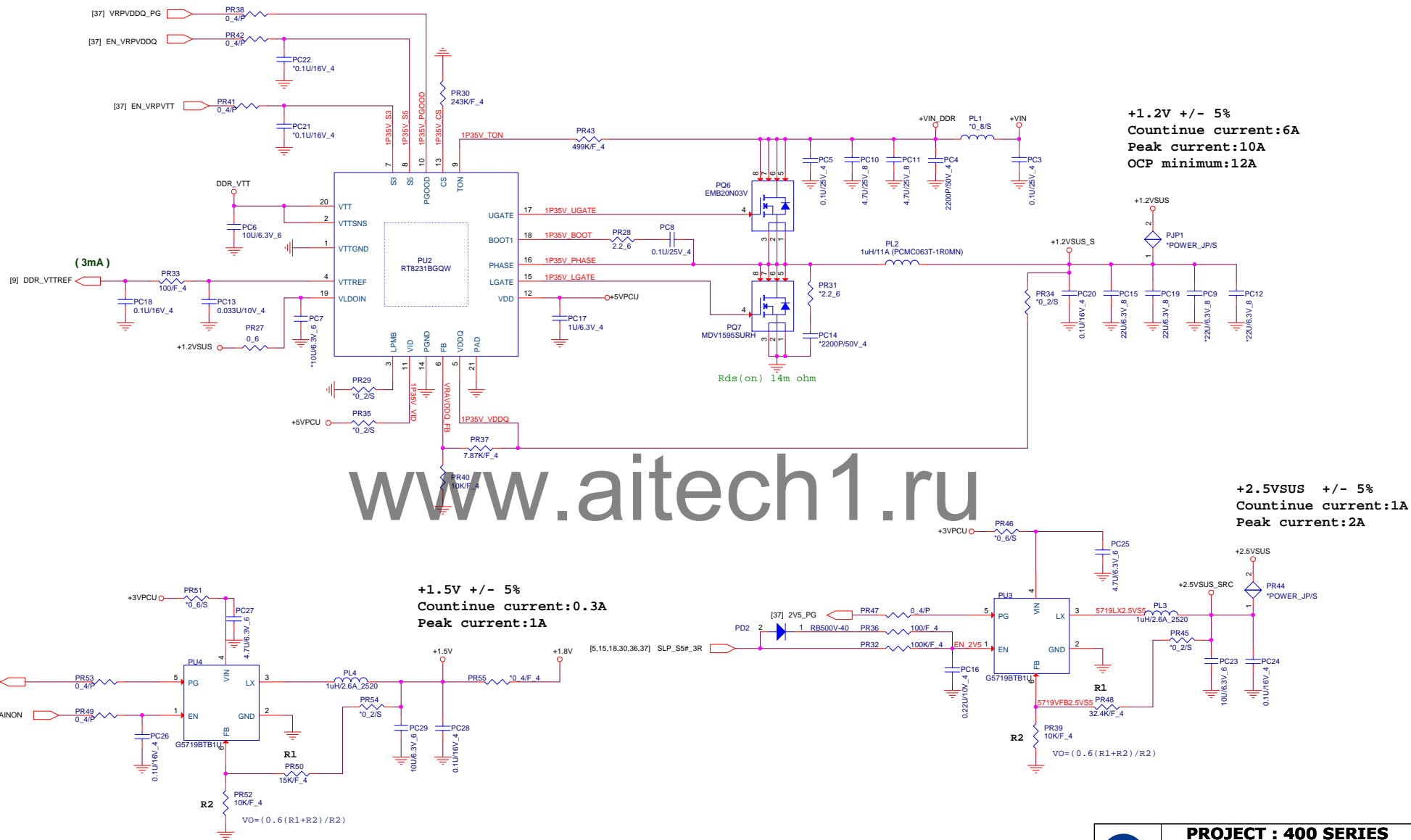


+3VPCU [7,19,22,23,24,27,28,29,34,35,36,37,38,40,42,47,48]
+5VPCU [15,18,19,20,38,40,41,42,43,45,47,49]

+5VPCU +/- 5%
Countinue current:9A
Peak current:11A
OCP minimum:13A

+3VPCU +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:10A







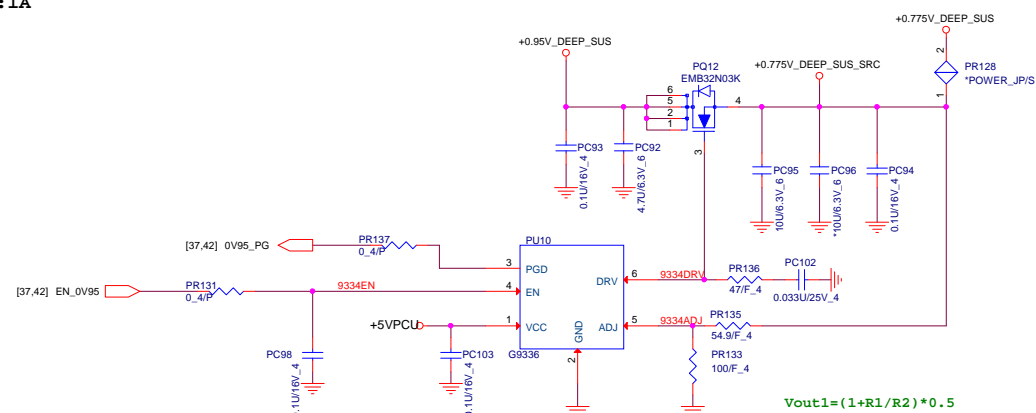
PC130 DP160

PROJECT : 400 SERIES

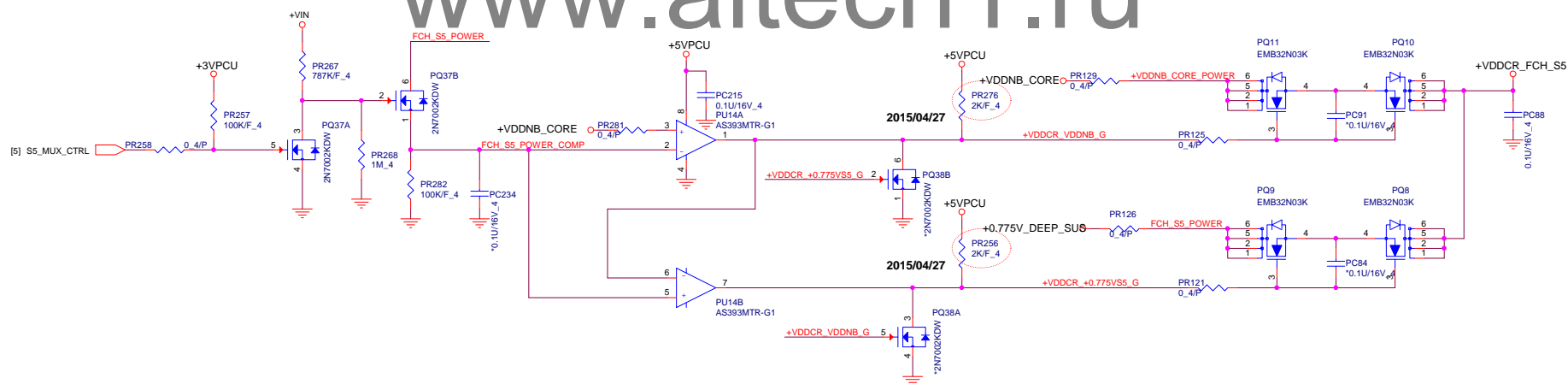


+3VPCU	7,19,22,23,24,27,28,29,34,35,36,37,38,39,40,42
+5VPCU	1,15,18,19,20,28,39,40,42,43,45,47,49

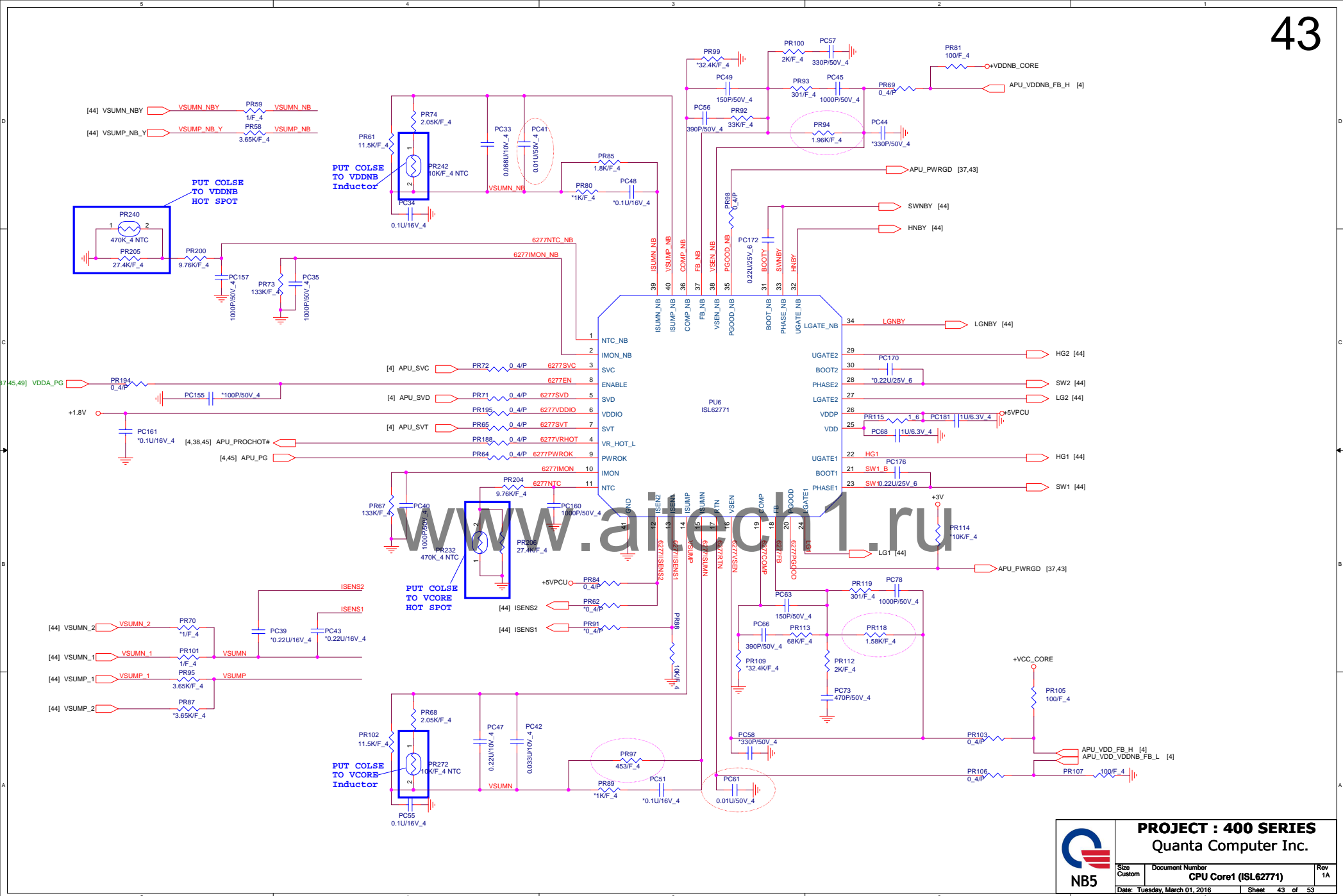
Quanta Computer Inc.

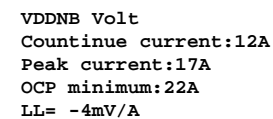
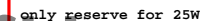
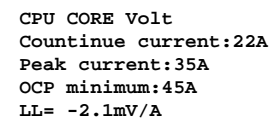


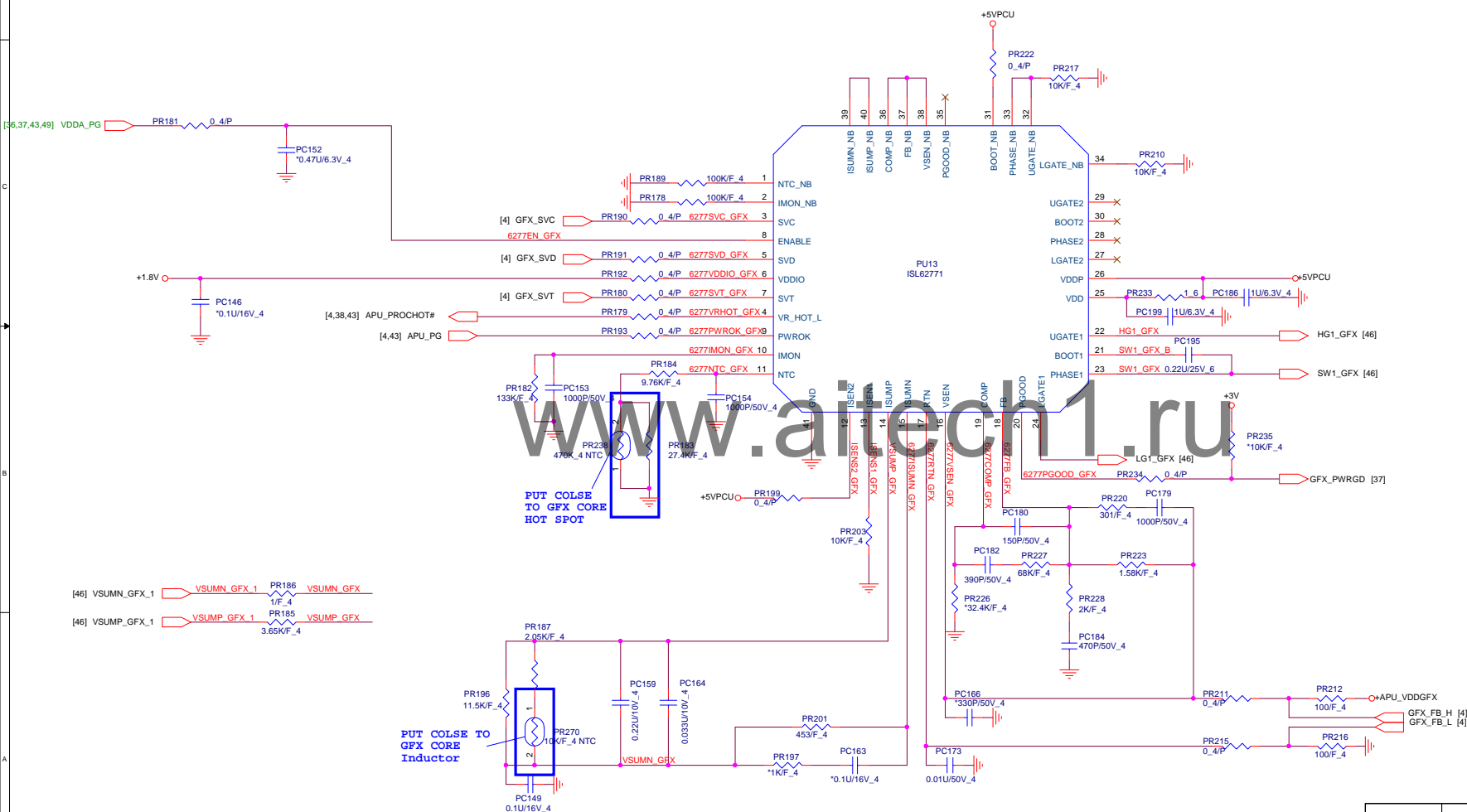
www.aitech1.ru

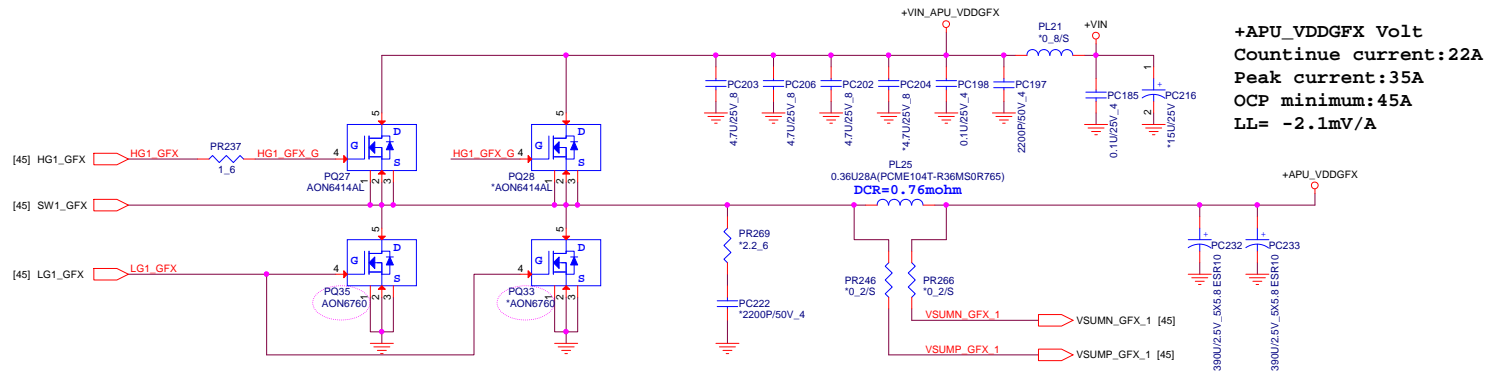


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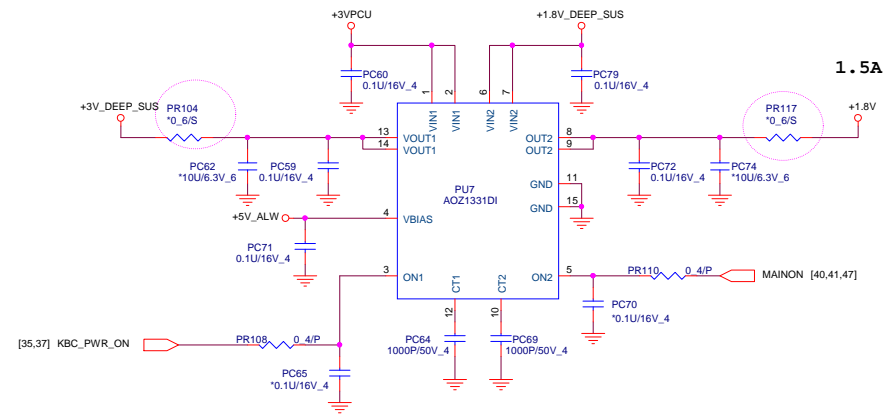
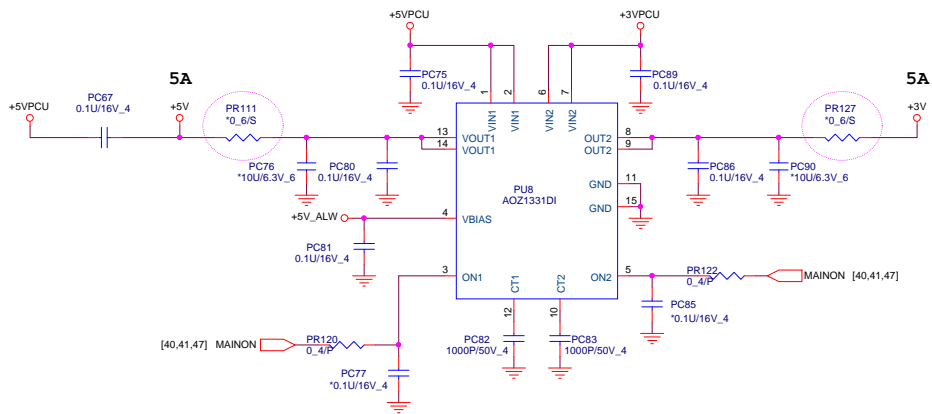






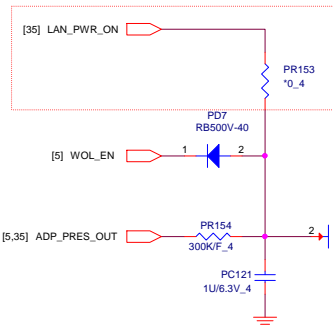


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Alfred@DB0, 1103,

1. HP requests to reserve the control the LAN Power from EC Side, so reserved R 0ohm and un-Stuff.

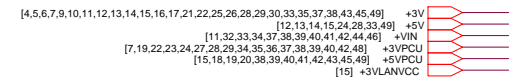
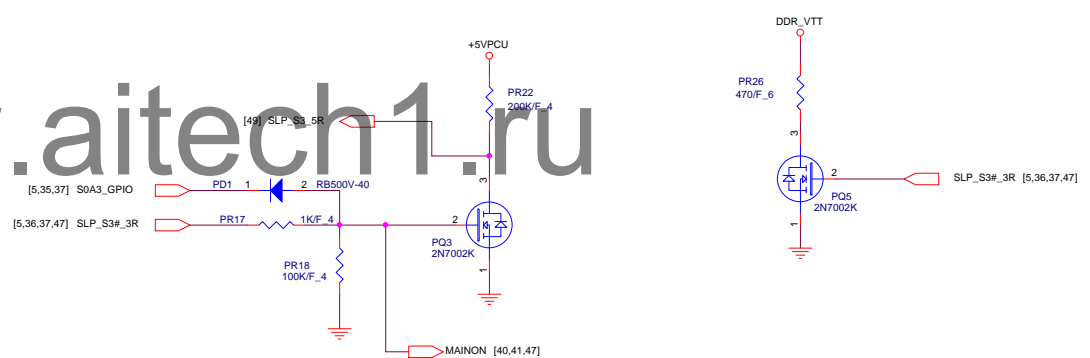



For WOL GPIO8

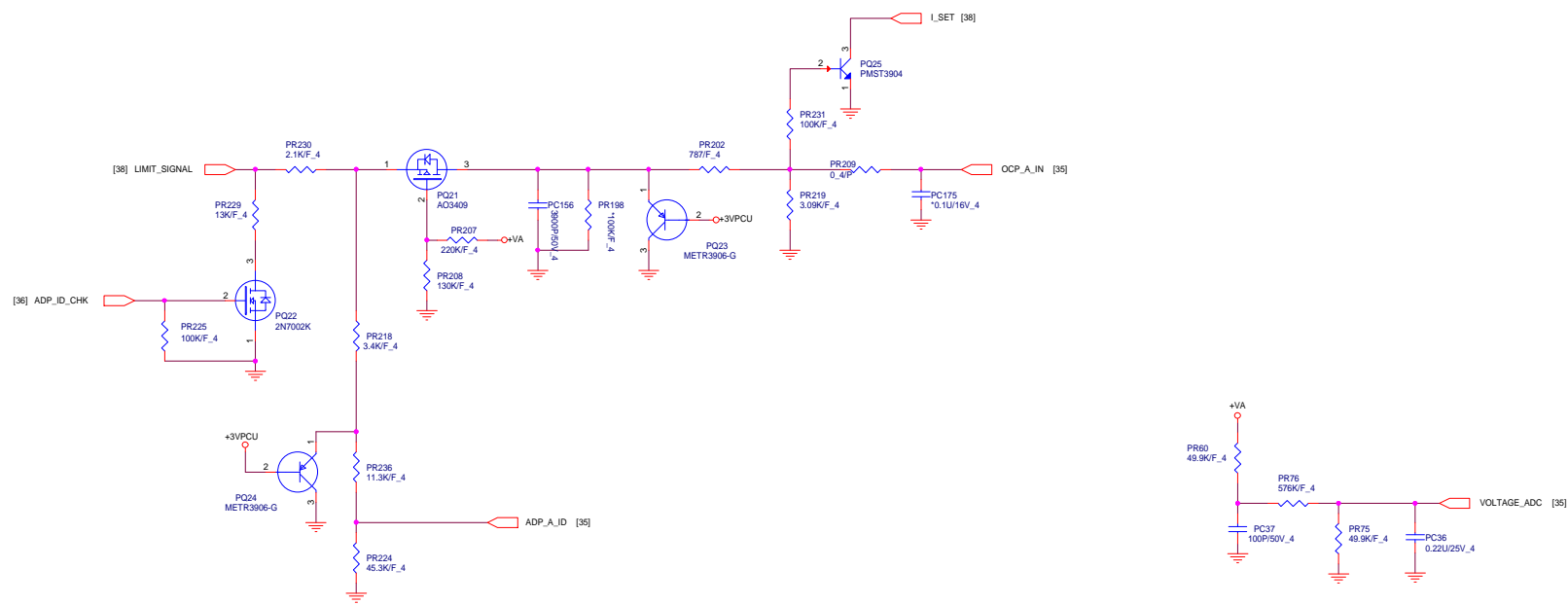
	Carrizo	Carrizo-L
PR102	2.2K	300K

Alfred@DB0, 1103,

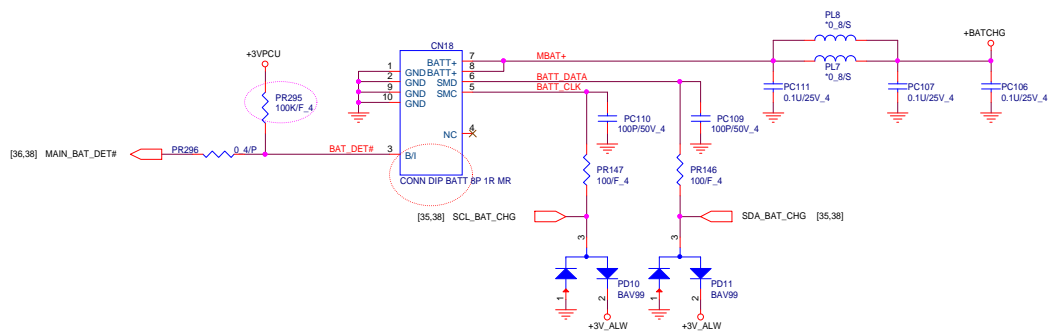
1. Dut to swap the WOL_EN from AGPIO7 to AGPIO8 and have a PU in EE side, it can use the 300K ohm both BR & ST APU.

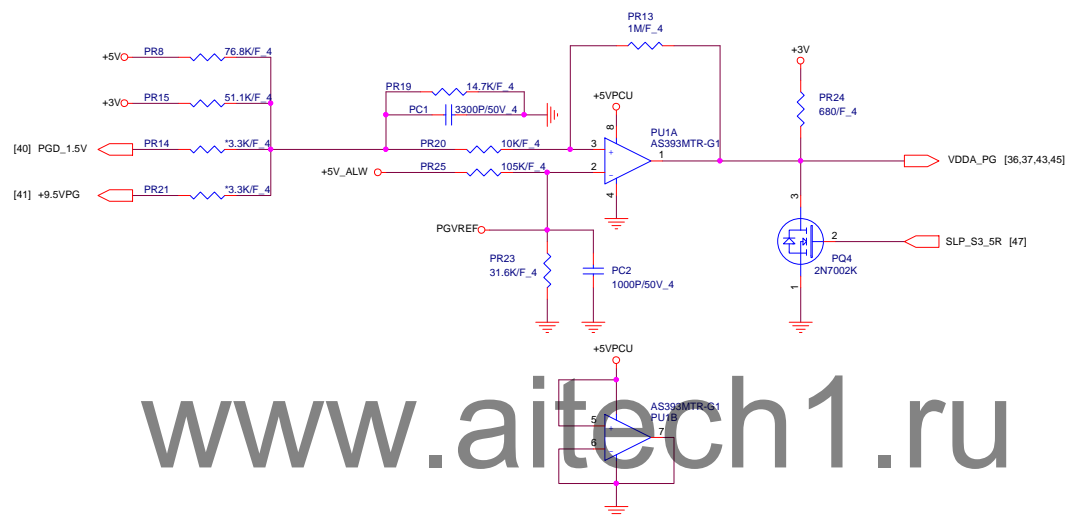


		PROJECT : 400 SERIES	
		Quanta Computer Inc.	
Size Custom	Document Number Dis-charge IC (SLG55448)	Rev 1A	
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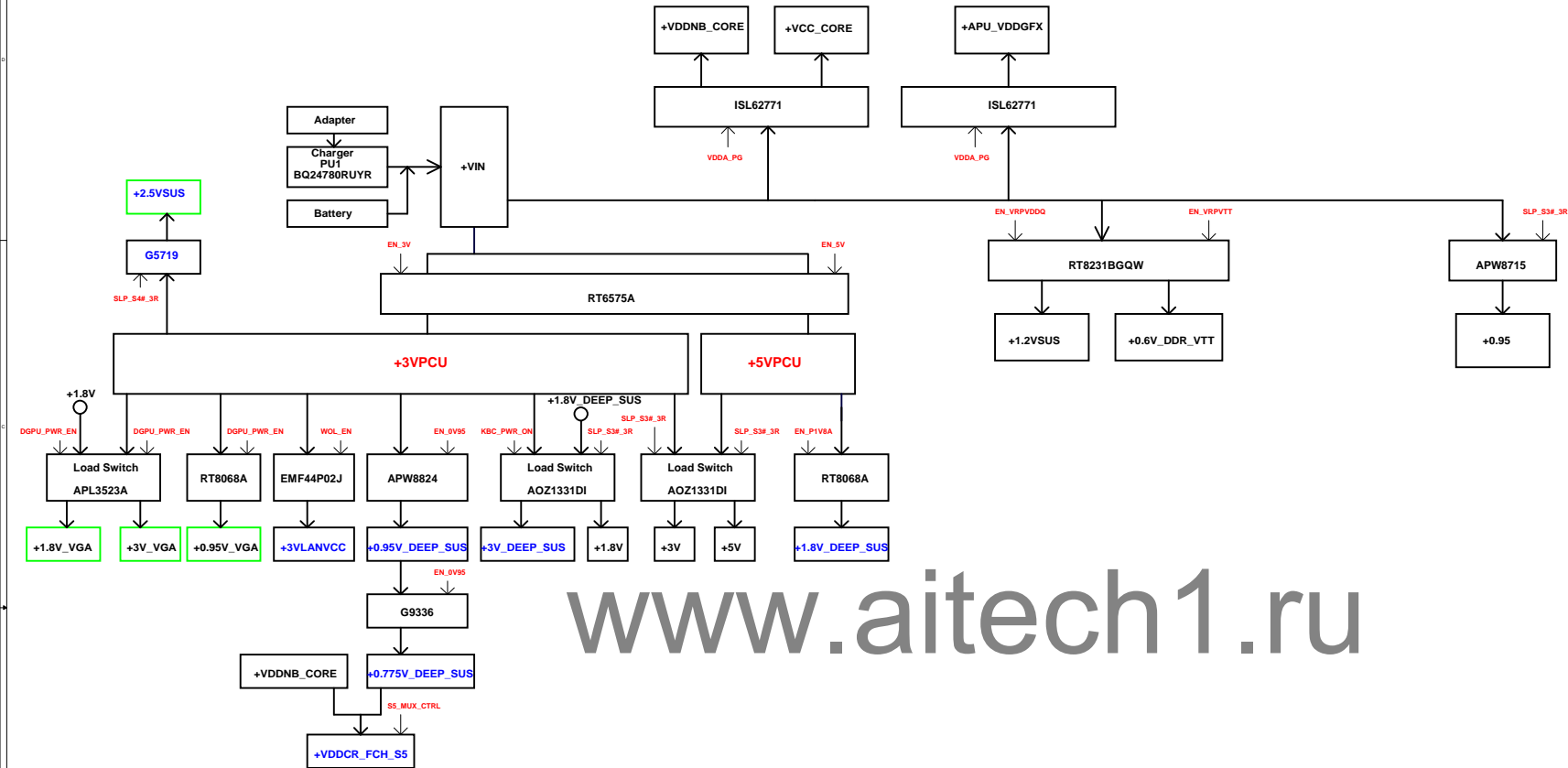


NB5

PROJECT : 400 SERIES
Quanta Computer Inc.

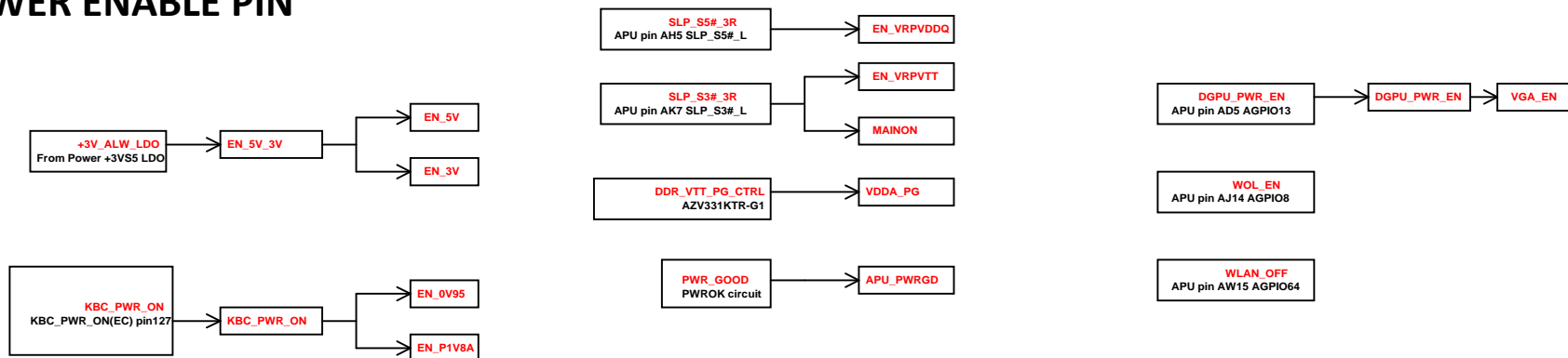
Size Custom	Document Number 56 --Power OK	Rev 1A
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POWER BLOCK DIAGRAM



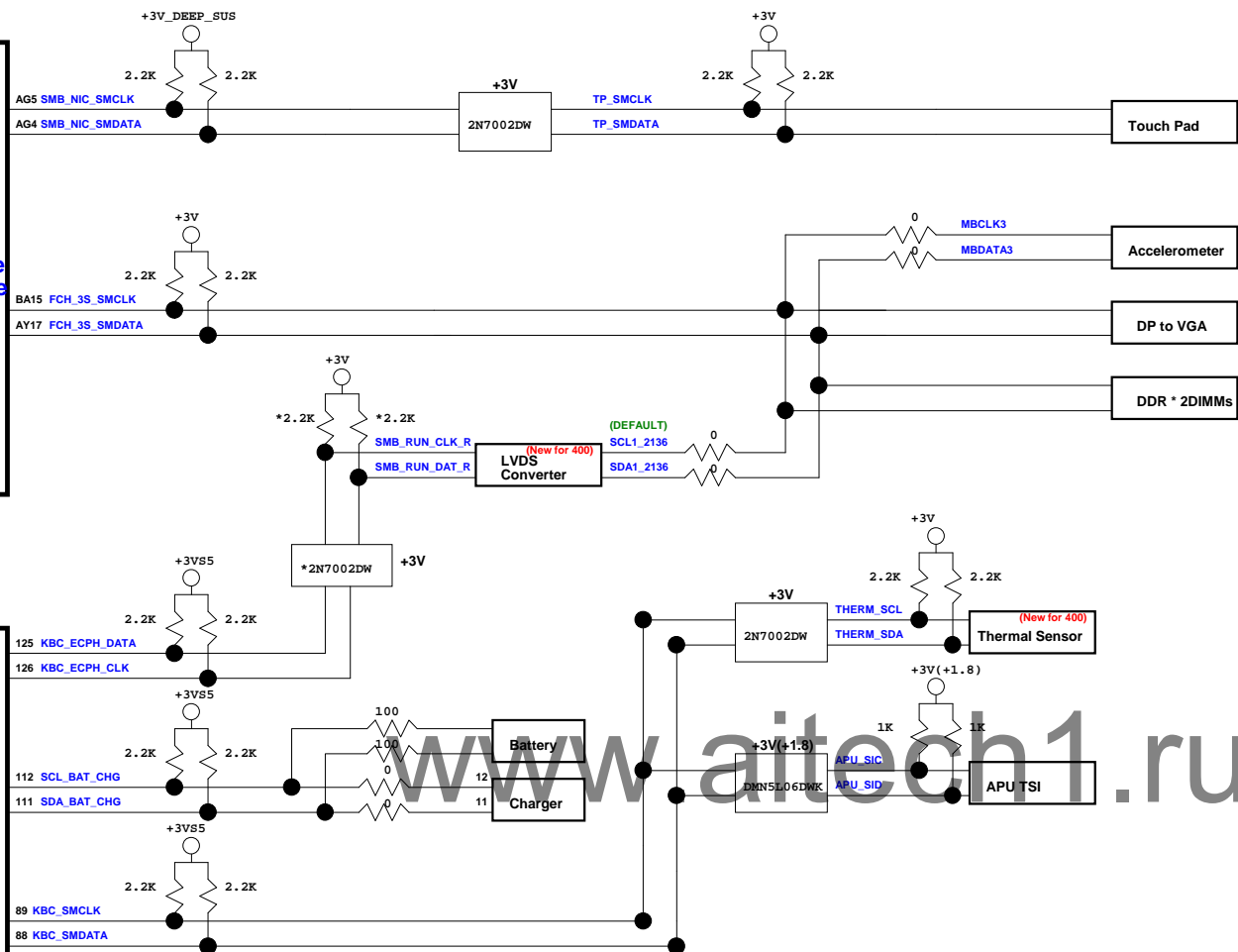
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POWER ENABLE PIN



Bristol Ridge
Stoney Ridge

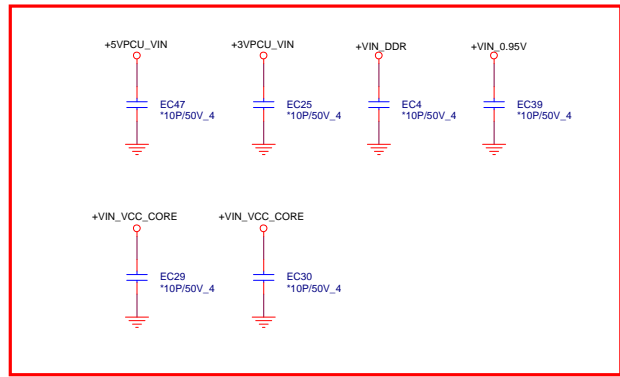
EC
NPCE586H



HSIO Lane	Port Assignment
USB3 #0	NC
USB3 #1	USB Type-C
USB3 #2	USB Type-C
USB3 #3	USB2.0/USB3.0 Combo Jack
PCIe0	NIC
PCIe1	WLAN
PCIe2	NC
PCIe4	Cardreader (PCIe)
DDI0	eDP
DDI1	DP2VGA
DDI2	HDMI
SATA0	HDD/ BOM 0 ohm Option for M.2 SSD
SATA1	ODD
PEG0~3	NC
PEG4~7	NC

USB2.0	Port Assignment
USB2 #0	Camera
USB2 #1	USB2.0(Right side on USB Board)
USB2 #2	USB2.0(Right side on USB Board)
USB2 #3	Bluetooth
USB2 #4	Finger Print
USB2 #5	USB Type-C
USB2 #6	USB Type-C
USB2 #7	USB2.0/USB3.0 Combo Jack

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